MOTOROLA

GM350

Mobile Radio

Service Manual

68P02924X30C

European Publications Department (RPG) Fleet, Hampshire, England
Issue: May 1997

CAUTION



ELECTROSTATIC SENSITIVE DEVICES

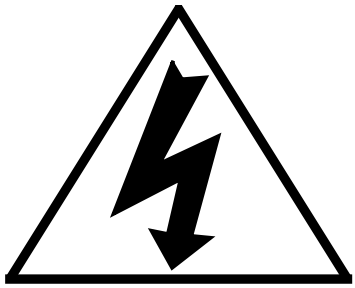
PRECAUTIONS SHOULD BE TAKEN TO MINIMIZE THE RISK OF DAMAGE BY ELECTROSTATIC DISCHARGE TO ELECTROSTATIC SENSITIVE DEVICES (ESDs).

ANY DEVICES EMPLOYING METAL OXIDE SILICON (MOS) TECHNOLOGY ARE PARTICULARLY SUSCEPTIBLE.

CIRCUIT DIAGRAMS MARKED WITH THE ABOVE SYMBOL INDICATE ELECTRONIC CIRCUITS (PECs) FOR WHICH ESD HANDLING PRECAUTIONS ARE NECESSARY.

THE USER SHOULD REFER TO BS5783, 1984: HANDLING OF ELECTROSTATIC SENSITIVE DEVICES. THIS BRITISH STANDARD SUPERSEDES DEF STAN 59-98, ISSUE 2.

WARNING



SAFETY WARNINGS

THE ELECTRICAL POWER USED IN THIS EQUIPMENT IS AT A VOLTAGE HIGH ENOUGH TO ENDANGER LIFE.

BEFORE CARRYING OUT MAINTENANCE OR REPAIR, PERSONS CONCERNED MUST ENSURE THAT THIS EQUIPMENT IS ISOLATED FROM THE ELECTRICAL SUPPLY AND TESTS ARE MADE TO ENSURE THAT ISOLATION IS COMPLETE.

WHEN THE SUPPLY CANNOT BE ISOLATED, MAINTENANCE AND REPAIR MUST BE UNDERTAKEN BY PERSONS WHO ARE FULLY AWARE OF THE DANGERS INVOLVED AND WHO HAVE TAKEN ADEQUATE PRECAUTIONS TO PROTECT THEMSELVES.

COMPONENTS CONTAINING BERYLLIUM OXIDE ARE USED IN THIS EQUIPMENT. DUST FROM THIS MATERIAL IS A HEALTH HAZARD IF INHALED OR ALLOWED TO COME INTO CONTACT WITH THE SKIN.

GREAT CARE MUST BE TAKEN WHEN HANDLING THESE COMPONENTS WHICH MUST NOT BE BROKEN OR SUBJECTED TO EXCESSIVE HEATING. DEFECTIVE COMPONENTS MUST BE DISPOSED OF IN ACCORDANCE WITH CURRENT INSTRUCTIONS.

LEAD ACID BATTERIES MAY BE FITTED AS THE STANDBY BATTERY. CARE MUST BE TAKEN WHEN REMOVING OR INSTALLING THESE BATTERIES TO:

1. ENSURE THAT THE TERMINALS ARE NOT SHORTED TOGETHER.

2. PREVENT SPILLAGE OF THE CORROSIVE ELECTROLYTE.

Service Manual

Contents

Chapter

1.0 Introduction

Gives a brief introduction into the manual and the service policy.

2.0 Model Chart and Accessories

Provides list of models and accessories available for the mobile radio.

3.0 Maintenance

Describes how to disassemble/assemble the radio for maintenance purposes and gives details on safety precautions. There is also information on testing/ servicing the radio using the front panel and diagnostics test modes.

4.0 Theory Of Operation

Gives a detailed description about the operation of the radio. The information is supplied to circuit reference detail.

5.0 Schematic Diagrams and Parts Lists

Provides component location diagrams, schematic diagrams and associated parts lists.

6.0 300-345MHz Band Specific Information

Provides all information concerning 300-345MHz band split including component location diagrams, schematic diagrams and associated parts lists.

7.0 66-88MHz Band Specific Information

Provides all information concerning Midband 66-88MHz band split including component location diagrams, schematic diagrams and associated parts lists.

Appendix

A.0 PL (CTCSS) Codes

B.0 External Device Connectors

C.0 Radio Conversions

Chapter 1

Introduction

Table of Contents

Paragraph		Page
1.0	**Introduction**	1
2.0	**Scope of Manual**	1
3.0	**How to Use This Manual**	1
4.0	**Warranty and Service Support**	1
4.1	Warranty Period	1
4.2	After Warranty	2
4.3	Piece Parts	2
4.4	Technical Support	2
5.0	**GM350 Technical Specification**	2
5.1	General	2
5.2	Transmitter	3
5.3	Receiver	3

1.0 Introduction

This chapter outlines the scope and use of the service manual and provides an overview of the warranty and service support. The radio specifications are also supplied in this chapter.

2.0 Scope of Manual

This manual is intended for use by experienced technicians familiar with similar types of equipment. It contains service information required for the equipment described and is current as of the printing date. Changes which occur after the printing date are incorporated by a complete Service Manual revision to your Product Manual.

3.0 How to Use This Manual

This manual contains introductory material such as overview, model charts, specifications and accessories and the remaining chapters deal with specific service aspects of the radio.
Refer to the Table of Contents for a general overview of the manual.

4.0 Warranty and Service Support

Motorola offers long term support for its products. This support includes full exchange and/or repair of the product during the warranty period, and service/ repair or spare parts support out of warranty. Any "return-for-exchange" or "return-for-repair" by an authorised Motorola Dealer must be accompanied by a Warranty Claim Form. Warranty Claim Forms are obtained by contacting an Authorised Motorola Dealer.

4.1 Waranty Period

The terms and conditions of warranty are defined fully in the Motorola Dealer or Distributor or Reseller contract. These conditions may change from time to time and the following notes are for guidance purposes only.

In instances where the product is covered under a "return for replacement" or "return for repair" warranty, a check of the product should be performed prior to shipping the unit back to Motorola. To ensure the product has been correctly programmed or has not been subjected to damage outside the terms of the warranty.

Prior to shipping any radios back to the appropriate Motorola warranty depot, please contact Customer Services. All returns must be accompanied by a Warranty Claim Form, available from your Customer Services representative. Products should be shipped back in the original packaging, or correctly packaged to ensure no damage occurs in transit.

4.2 After Warranty Period

After Warranty period, Motorola continues to support products in two ways. Firstly, Motorola's Radio Parts and Service Group (RPSG) offer a repair service to both end users and dealers at competitive prices. Secondly, RPSG supplies individual parts and modules that can be purchased by dealers who are technically capable of performing fault analysis and repair.

4.3 Piece Parts

Some replacement parts, spare parts, and/or product information can be ordered directly. If a complete Motorola part number is assigned to the part, it is available from Motorola Radio Parts and Service Group (RPSG). If a generic part is listed or only a part description is listed, the part is not normally available from Motorola. If a parts list is not included, this generally means that no user-serviceable parts are available for that kit or assembly. All orders for parts/information should include the complete Motorola identification number. All part orders should be directed to your local RPSG office.

Head Office
Motorola G.m.b.H.
European Parts Department
65232 Taunusstein
Germany

4.4 Technical Support

Motorola Product Services is available to assist the dealer/distributors in resolving any malfunctions which may be encountered. Initial contact should be by telephone whenever possible. When contacting Motorola Technical Support, be prepared with the product model number and the unit's serial number.

5.0 GM350 Technical Specification

5.1 General

SPECIFICATION ITEM	TYPICAL VALUE
Frequency Range	VHF: 136-174 MHz UHF: 403-470 MHz
Channel Spacing	12.5 or 20/25 kHz
Frequency Stability	±2ppm(UHF); ±5ppm (VHF)
Power Supply	10.8 to 15.6V dc, negative earth
Dimensions	44x168x160 mm (HxWxD)
Weight	1030g
Operational Temperature	- 25°C to + 55°C
Storage Temperature	- 40°C to + 85°C
Antenna Connection	50Ω BNC
Environmental - Mechanical - Electrical	 Vibration IEC 68/2/27 and Shock IEC 28/2/6 European Dust & Water protection IP54 ETS300-086 RF Specifications ETS300-113 Cyclic Keying Requirements ETS300-279 EMC Requirements ETS300-219 Signalling

5.2 Transmitter

SPECIFICATION ITEM	TYPICAL VALUE
Channel Spacing	12.5 or 20/25 kHz
Output Power	5-25W
Modulation Limiting	<±2.5kHz (12.5kHz); <±4kHz (20kHz); <±5kHz (25kHz)
FM hum & noise (CCITT)	>40dB (12.5kHz); >45dB (25kHz) CCITT
Conducted/Radiated Emission	<0.25uW (0.1...1000MHz); <1uW (1...4GHz)
Adjacent Channel Power	<-60dB (12.5kHz); <-70dB (25kHz)
Audio Response (300 - 3000 Hz)	Flat or pre-emphasised
Audio Distortion	<5% @ 1kHz, 60% deviation
Transmit turn on time	<25msec

5.3 Receiver

SPECIFICATION ITEM	TYPICAL VALUE
Channel Spacing	12.5 or 20/25 kHz
Sensitivity @ 12.5 kHz	< 0.35uV (12dB SINAD)
Sensitivity @ 25 kHz	< 0.35uV (12dB SINAD)
Intermodulation	>65dB ETS; >70dB with Base Option
Adjacent Channel Selectivity	>60dB (12.5kHz); >70dB (20/25kHz) ETS
Spurious Rejection	>70dB ETS
Audio Distortion @ Rated Audio	<5%
Hum and Noise (CCITT)	>40dB (12.5kHz); >45dB (20/25kHz) CCITT
Audio Response (300 - 3000 Hz)	Flat or De-Emphasised
Co-channel Rejection	<12dB (12.5kHz) , <8dB (20/25kHz) ETS
Conducted /Radiated Emission	<2nW (0,1..1000MHz); <20nW (1..4GHz)
Receive after transmit time	<25msec
Audio Output Power	4W (internal speaker); <13W external

Chapter 2

Model Chart and Accessories

Table of Contents

Paragraph		Page
1.0	**Overview**	1
2.0	**Model Chart**	1
3.0	**Accessories**	2
3.1	Mechanical Hardware Kits	2
3.2	Microphones	2
3.3	Speakers	2
3.4	Cables	2
3.5	Other	2

1.0 Overview

This chapter lists the models and accessories available for the GM350 mobile radio.

2.0 Model Chart

Description	GM350 136-174 MHz 12.5 kHz 25W	GM350 136-174 MHz 12.5 kHz 25W D	GM350 136-174 MHz 20/25 kHz 25W	GM350 136-174 MHz 20/25 kHz 25W D	GM350 403-470 MHz 12.5 kHz 25W	GM350 403-470 MHz 12.5 kHz 25W D	GM350 403-470 MHz 20/25 kHz 25W	GM350 403-470 MHz 20/25 kHz 25W D	**GM350 136-174 MHz VHF 403-470 MHz UHF** X = Indicates one of each required	
Model	M08KHE4AA2AN	M08KHF4AA3AN	M08KHE6AA2AN	M08KHF6AA3AN	M08RHE4AA2AN	M08RHF4AA3AN	M08RHE6AA2AN	M08RHF6AA3AN		
									Item	**Description**
	X	X	X	X	X	X	X	X	GBN6147	Packaging Kit
	X		X		X		X		GCN6103	Control Head Model A2 Non-Display
		X		X		X		X	GCN6105	Control Head Model A3 Display
	X	X	X	X	X	X	X	X	GLN7324	Low Profile Trunnion Kit
	X	X	X	X	X	X	X	X	GMN6146	Enhanced Compact Microphone
					X				GUE1118	RF & HSG UHF 4ch 12.5kHz 5-25W
							X		GUE1119	RF & HSG UHF 4ch 20/25kHz 5-25W
	X								GUD1304	RF & HSG VHF 4ch 12.5kHz 5-25W
			X						GUD1305	RF & HSG VHF 4ch 20/25kHz 5-25W
						X			GUE1116	RF & HSG UHF 128ch 12.5kHz 5-25W
								X	GUE1117	RF & HSG UHF 128ch 20/25kHz 5-25W
		X							GUD1302	RF & HSG VHF 128ch 12.5kHz 5-25W
				X					GUD1303	RF & HSG VHF 128ch 20/25kHz 5-25W
	X	X	X	X	X	X	X	X	GKN6270	Power Cable
	X	X	X	X	X	X	X	X	68P02923X01	GM350 User Guide M/L
	X	X	X	X	X	X	X	X	68P02931X01	BZT Certificate (Germany Only)

3.0 Accessories

3.1 Mechanical Hardware Kits:

GLN7324	Low Profile Trunnion kit (Standard)
GLN7317	High Profile Trunnion kit
GLN7320	In-Dash Mount, DIN installation kit
HLN9457	Accessory Connector Facility Kit
GLN7325	IP54 seal, Accessory Connector

3.2 Microphones:

GMN6146	Enhanced Compact Microphone (Standard)
GMN6148	DTMF Microphone
HMN3141	Handset, low cost with Hang-up cup
HMN3000	Desk Microphone

3.3 Speakers:

All speaker connecting cables have 16-pin accessory connector plug.

GSN6059	13W External Speaker, square

3.4 Cables:

GKN6270	Battery power cable 3m, 10A fuse (Standard)
GKN6271	Ignition switch cable

3.5 Other:

GKN6272	External Alarm, Relay and Cable Kit
GLN7323	External PTT
GLN7318	Base Tray
GPN6126	24/12V DC Converter, 6A
GPN6127	24/12V DC Converter, 15A
GPN6133	EMC approved Power Supply
HPN4002	Non-EMC approved Power Supply
HPN8393	Non-EMC approved Power Supply

Chapter 3

Maintenance

Table of Contents

Paragraph		Page
1.0	**Overview**	1
2.0	**Disassemble the Radio**	1
2.1	Remove the Control Head	1
2.2	Remove the Top Cover	1
2.3	Remove the Transceiver Board	2
2.4	Disassemble the Control Head	2
3.0	**Assemble Radio**	3
3.1	Assemble the Control Head	3
3.2	Replace the Transceiver Board	3
3.3	Replace the Top Cover and Control Head	3
4.0	**Exploded View Diagrams and Parts**	4
5.0	**Service Aids**	6
6.0	**Test Equipment**	7
7.0	**Radio Tuning Procedure**	8
7.1	General	8
7.2	PA Bias Voltage	9
7.3	Battery Threshold	10
7.4	Transmitter Power	10
7.5	Reference Oscillator	11
7.6	Front-End Pre-Selector	11
7.7	Rated Volume	12
7.8	Squelch	12
7.9	Transmit Deviation Limit	13
7.10	Transmit Modulation Balance (Compensation)	14

1.0 Overview

This chapter explains, step by step, how to disassemble and assemble the radio, to transceiver board level. The chapter also contains a list of test equipment required to service the radio. The procedure for radio alignment and the test setup is also available in this chapter.

2.0 Disassemble the Radio

2.1 Remove the Control Head

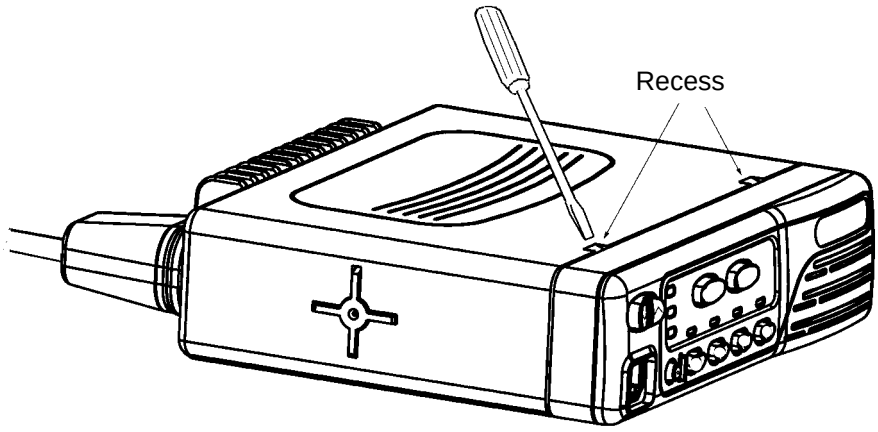


Figure 3-1 Control Head Removal.

1. Insert a small flat blade screw driver, or similar, in the recess between the control head and the transceiver (to minimise cosmetic damage to the radio cover start from the bottom side).
2. Press until the side of the control head releases and then repeat the operation on the opposite side of the radio.
3. Pull the control head away from the transceiver.
4. Remove the flex from the socket on the control head board.

2.2 Remove the Top Cover

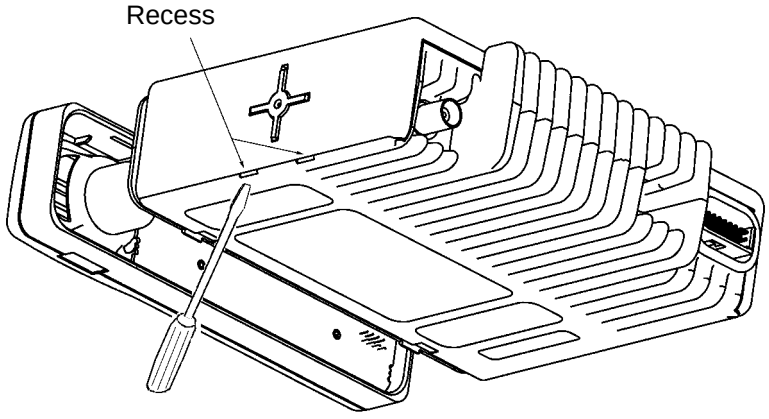


Figure 3-2 Top Cover Removal.

1. Insert a small flat blade screw driver in the side recess of the radio chassis.
2. Lift the top cover over the chassis.

2.3 Remove the Transceiver Board

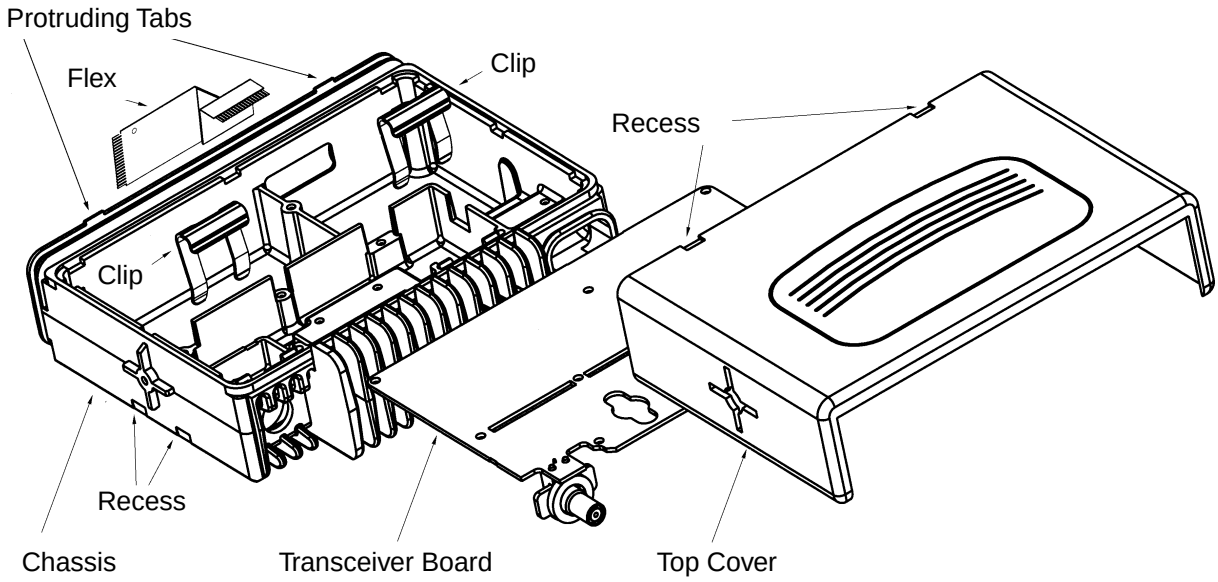


Figure 3-3 Transceiver Board Removal.

1. Remove the power and antenna connector retaining clips by inserting a small flat blade screw driver between the clip and the top of the chassis wall and gently prying the clip upwards.
2. Remove 13 screws from the transceiver board using a T8 TORX driver.
3. Carefully remove the transceiver board by rotating it out of the chassis:

   Slowly lift the board on the front edge, the side with the connector that mates with the control head, and pull gently toward the front of the radio.

CAUTION: The thermal grease can act as an adhesive and cause the leads of the heat dissipating devises to be over stressed if the board is lifted too quickly.



2.4 Disassemble the Control Head

1. To pull out the printed circuit board from the control head housing, insert a small blade screw driver in the side groove near the four protruding tabs. Remove the board from the control head housing.
2. Disconnect the board from the speaker by removing from the socket.
3. Remove the keypad from the control head housing by lifting up the rubber keypad. Care should be taken not to touch or get other contaminates on the conductive pads on the under side of the keypad or conductive contacts on the printed circuit board.

3.0 Assemble Radio

3.1 Assemble the Control Head

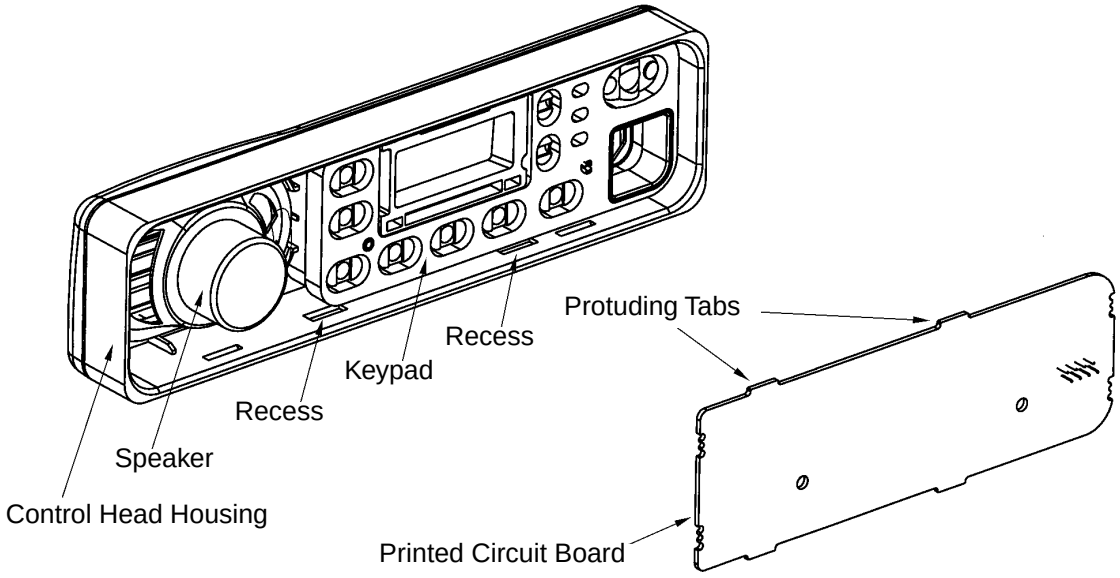


Figure 3-4 Control Head Assembly.

1. Place the keypad onto the board assembly, making sure the keypad is flush with the board.
2. Make sure the speaker including the gasket is well positioned.
3. Connect the printed circuit board to the speaker.
4. During the installation of the printed circuit board, ensure the four protruding tabs snap into the recesses.

3.2 Replace the Transceiver Board

1. Inspect and if necessary, reapply thermal grease to the heatsinking pads in the chassis.
2. Before installing the connector retaining clips, ensure that the board is sitting flush on the chassis mounting surface.
3. Install the 13 screws with 0.4 -07 NM (4-6 in lbs) of torque using a T8 TORX driver.

3.3 Replace the Top Cover and Control Head

1. Position the top cover over the chassis and replace. Ensure that the cross snaps into the recesses.
2. Connect the control head to the radio by the flex.
3. Press the control head onto the radio chassis until the protruding tabs on the chassis snap into the recesses inside the control housing, see Figure 3-5.

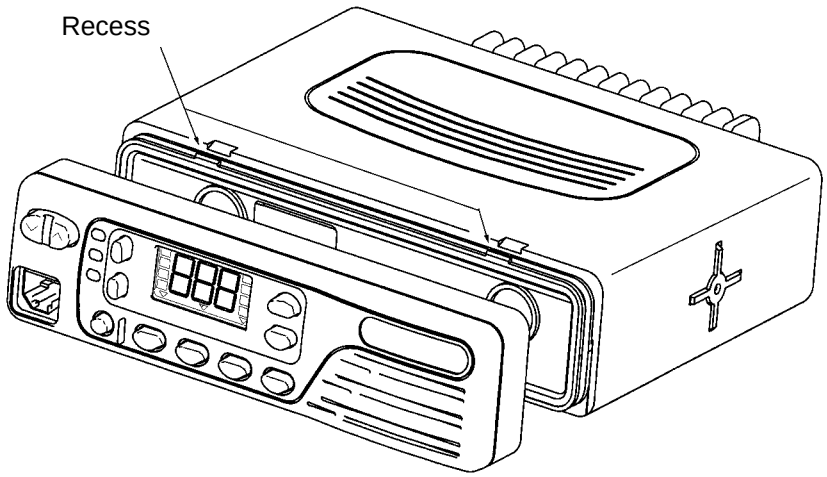


Figure 3-5 Control Head Replacement.

4.0 Exploded View Diagrams and Parts

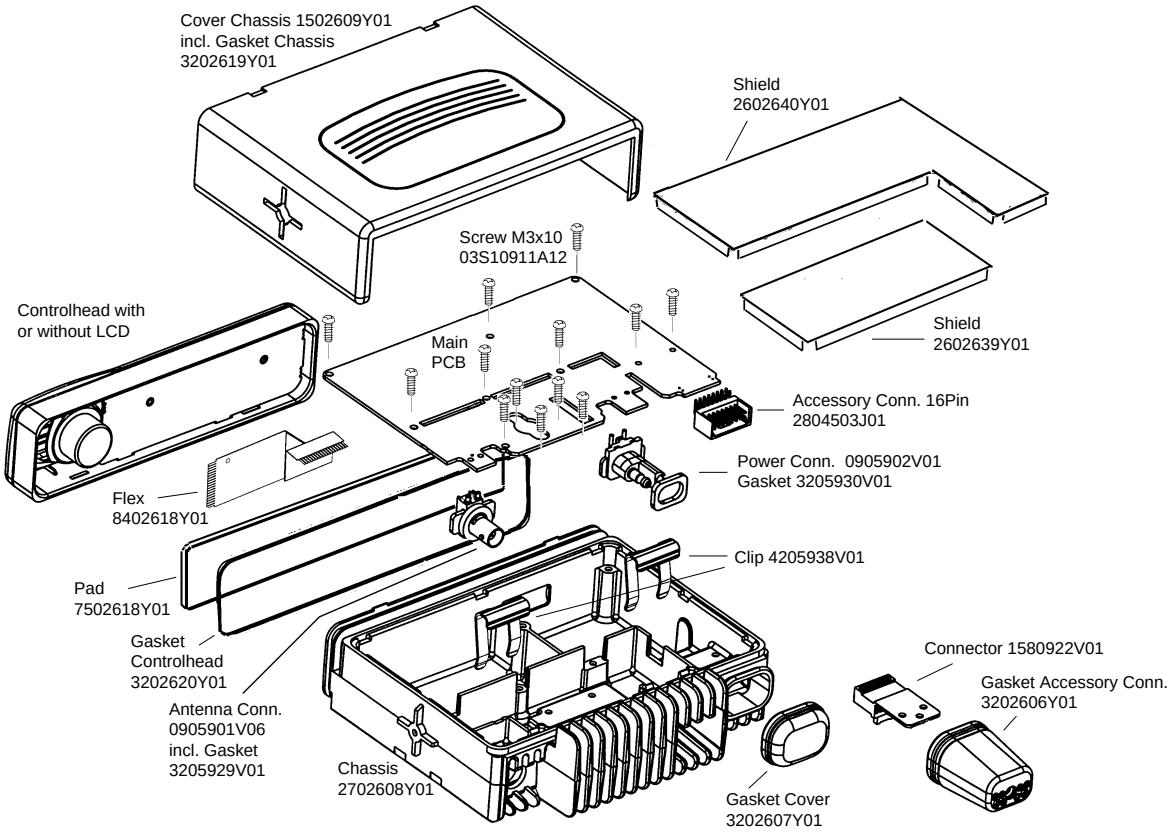


Figure 3-6 Radio Exploded View Diagram.

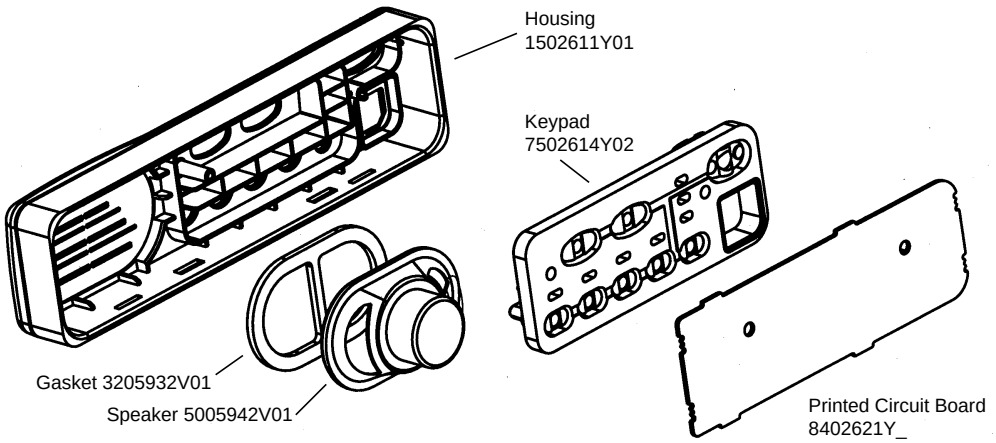


Figure 3-7 Control Head Model A2.

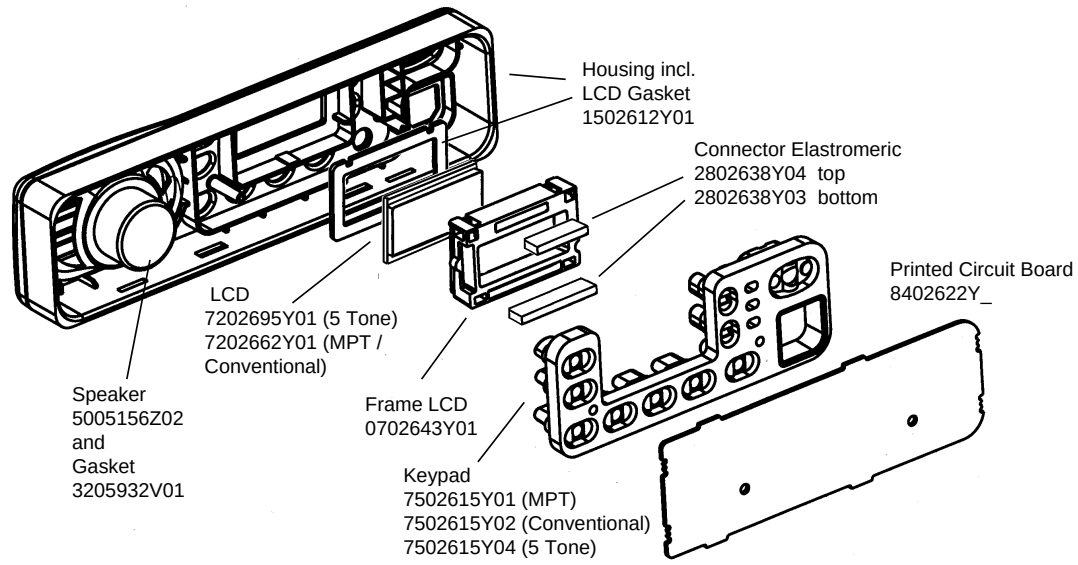


Figure 3-8 Control Head Model A3.

5.0 Service Aids

The list in table 3-1 includes service aids recommended for working on the GM350 radio.

Table 3-1 Service Aids.

PART No.	DESCRIPTION	APPLICATION
GTF376	Test Box Cable	Connects radio to GTF180 test box.
GTF374	Combined Interface Cable	Connects radio to RLN4008 RIB.
GPN6133	Power Supply	Used to supply power to the radio.
GKN6266	DC Power Cable for radio	Interconnects radio to power supply.
GTF180	Test Box	Enables connection to the universal connector. Allows switching for radio testing.
RLN4008	Radio Interface Box	Enables communications between the radio and the computer's serial communications adapter.
EPN4040	Power Supply	Used to supply power to the RIB (240 VAC).
EPN4041	Power Supply	Used to supply power to the RIB (220 VAC).
3080369B72	Computer Interface Cable	Connects the computer's serial communications adapter (9 pin) to the RIB.
3080369B71	Computer Interface Cable	Connects the computer's serial communications adapter (25 pin) to the RIB.

6.0 Test Equipment

The list in table 3-2 includes all standard test equipment required for servicing two-way mobile radios, as well as several unique items designed specifically for servicing the GM350 radio. Battery-operated test equipment is recommended when available. The “Characteristics” column is included so that equivalent equipment may be substituted; however, when no information is provided in this column, the specific Motorola model listed is either a unique item or no substitution is recommended.

Table 3-2 Recommended Test Equipment.

MODEL No.	DESCRIPTION	CHARACTERISTICS	APPLICATION
R2000 Series	System Analyser	This monitor will substitute for items with an asterisk (*)	Frequency/deviation meter and signal generator for wide-range troubleshooting and alignment.
*R1150C	Code Synthesizer		Injection of audio and digital signalling codes
*S1053D *HM-203-7 *SKN6008A *SKN6001A	220 VAC Voltmeter 110 VAC Voltmeter Power Cable for Meter Test Leads for Meter	1mV to 300V, 10MΩ Input impedance	Audio voltage measurements
*S1350C *ST1213B (VHF) *ST1223B (UHF)	Watt Meter Plug-in Element RF Dummy Load	50 ohm, ±5% accuracy 10 Watts, maximum 0-1000 MHz, 300W	Transmitter power o/p measurements
R1065A	Load Resistor	10-watt Broadband	For use with Wattmeter
S1339A	RF Millivolt Meter 10kHz to 1.2 GHz	100µV to 3V RF	RF level measurements
*R1013A	SINAD Meter		Receiver sensitivity measurements
S1347D or S1348D (programmable)	DC Power Supply	0-20Vdc, 0-5 Amps	Bench supply for 13.2Vdc current limited

* Any of the R2000 Series system analysers will substitute for items with an asterisk (*)

7.0 Radio Tuning Procedure

7.1 General

The recommended hardware platform is a 386 or 486 DX 33 PC (personal computer) with 8 MBytes RAM, MS DOS 5.0, Windows 3.1, and RSS (Radio Service Software). These are required to align the radio. Refer to your RSS Installation Manual for installation and setup procedures for the required software; the user manual is accessed (and can be printed if required) via the RSS.

To perform the alignment procedures, the radio must be connected to the PC, RIB (Radio Interface Box), and Universal Test Set as shown in figure 3-9.

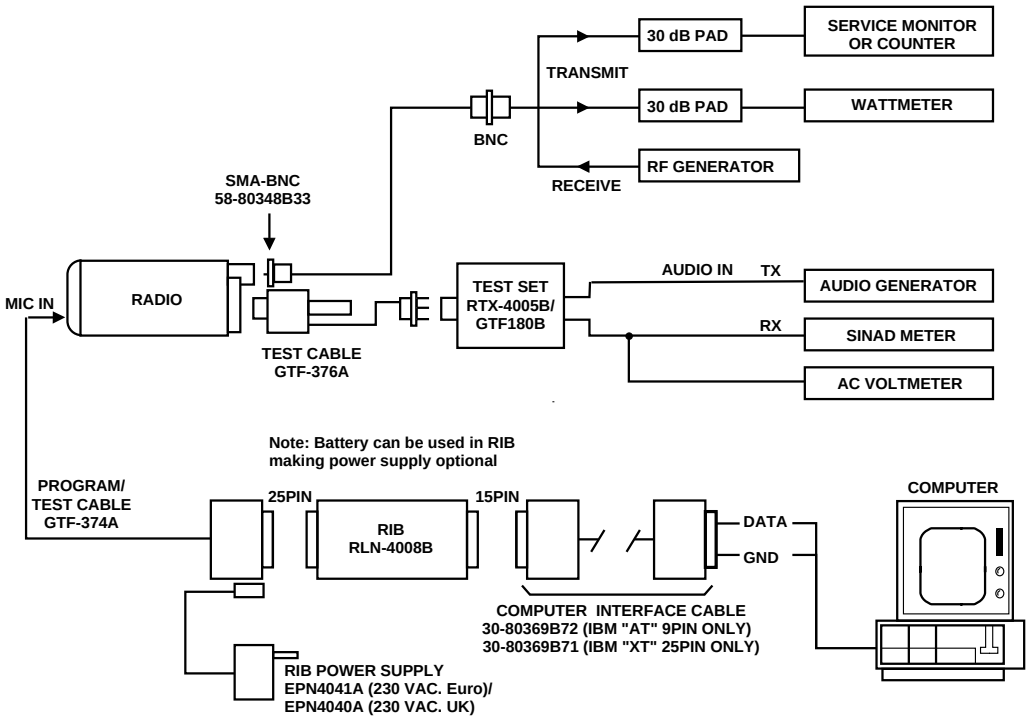


Figure 3-9 Radio Alignment Test Setup.

All tuning procedures are performed from the Service menu.

Before going into the Service menu, the radio must first be read using the File / Read Radio menu (if the radio has just been programmed with data loaded from disk or from a newly created codeplug, then it must still be read so that the RSS will have the radio's actual tuning values).

All Service windows read and program the radio codeplug directly; you do NOT have to use the RSS Read Radio / Write Radio functions to program new tuning values.

CAUTION: **DO NOT** switch radios in the middle of any Service procedure. Always use the Program or Cancel key to close the tuning window before disconnecting the radio. Improper exits from the Service window may leave the radio in an improperly configured state and result in seriously degraded radio or system performance.

The Service windows introduce the concept of the “Softpot”, an analog SOFTware controlled POTentiometer used for adjusting all transceiver alignment controls. A softpot can be selected by clicking with the mouse at the value or the slider or by hitting the TAB key until the value or the slider is highlighted.

Each Service window provides the capability to increase or decrease the ‘softpot’ value with the mouse, the arrow keys or by entering a value with the keyboard. The window displays the minimum, maximum, and step value of the softpot. In addition transmitter tuning windows indicate the transmitter frequency and whether the radio is keyed.

Adjusting the softpot value sends information to the radio to increase (or decrease) a DC voltage in the corresponding circuit. For example, increasing the value in the Reference Oscillator tune window instructs the radio microprocessor to increases the voltage across a varactor in the reference oscillator to increase the frequency. Pressing the Program button stores all the softpot values of the current window permanently in the radio.

In ALL cases, the softpot value is just a relative number corresponding to a D/A (Digital-to-Analog) generated voltage in the radio. All standard measurement procedures and test equipment are similar to previous radios.

Refer to the RSS on-line help for information on the tuning software.

Perform the following procedures in the sequence indicated.

Note: All tuning procedures must be performed at a supply voltage of 13.2V unless otherwise stated. The Modulation Analyser to measure the deviation should be set to frequency modulation with de-emphasis switched off and all high pass filters switched off.

7.2 PA Bias Voltage

Adjustment of the PA Bias is critical for proper radio operation. Improper adjustment will result in poor operation and may damage the PA FET device. For this reason, the PA bias must be set before the transmitter is keyed the first time.

1. From the Service menu, select Tx Alignment.
2. Select Bias Voltage to open the bias voltage tuning window. If the control voltage is out of range, an error message will be displayed. In this case the radio hardware has a problem and tuning must be stopped immediately.
3. Press the Toggle Bias button to set the quiescent current temporarily to 0 mA. The status bar will indicate that the bias is switched off.
4. Measure the DC current of the radio. Note the measured value and add the specified quiescent current shown in table 3-3. The result is the tuning target.
5. Press the Toggle Bias button to switch on the quiescent current again.
6. Adjust the current per the target calculated in step 4.
7. Press Program to store the softpot value.

Table 3-3 Quiescent Current Alignment.

RF-Band	Target
UHF	440mA±10%
VHF	150mA±15%

7.3 Battery Threshold

The radio uses 2 battery threshold levels Tx High and Tx Low to determine the battery condition.

1. From the Service menu, select Tx Alignment.
2. Select Battery Thresholds to open the battery thresholds tuning window.
3. Set the supply voltage to the value indicated for Tx High.
4. Press the Tx High Program button to store the softpot value for Tx High.
5. Set the supply voltage to the value indicated for Tx Low.
6. Press the Tx Low Program button to store the softpot value for Tx Low.
7. Close the window by pressing Cancel.

7.4 Transmitter Power

IMPORTANT: To set the transmitter power for customer applications use the Per Radio window under the Edit menu and set the “Level 1” and “Level 2” powers to the desired values. Only if the transmitter components have been changed should the following procedure be performed.

The advanced power setting technology employed in the GM350 makes use of two reference power level settings along with parameters describing the circuit behaviour. To set the reference points requires tuning on two power level settings, a high power level setting, and a low power level setting.

1. From the Service menu, select Tx Alignment.
2. Select RF Power to open the RF power tuning window. The window will indicate the transmit test frequencies to be used.
3. Select Point 1 value of the first frequency.
4. Press Toggle PTT to key the radio. The status bar will indicate that the radio is transmitting.
5. Measure the transmitter power on your power meter.
6. Enter the measured value in the box Point 1.
7. Select Point 2 value of the first frequency.
8. Measure the transmitter power on your power meter.
9. Enter the measured value in the box Point 2.
10. Press Toggle PTT to dekey the radio.
11. Repeat steps 3 - 10 for all test frequencies shown in the window.
12. Press Program to store the softpot values.

7.5 Reference Oscillator

Adjustment of the reference oscillator is critical for proper radio operation. Improper adjustment will not only result in poor operation, but also a misaligned radio that will interfere with other users operating on adjacent channels. For this reason, the reference oscillator should be checked every time the radio is serviced. The frequency counter used for this procedure must have a stability of 0.1 ppm (or better).

1. From the Service menu, select Tx Alignment.
2. Select Reference Oscillator to open the reference oscillator tuning window.
3. Press Toggle PTT to key the radio. The status bar will indicate that the radio is transmitting.
4. Measure the transmit frequency on your frequency counter.
5. Adjust the reference oscillator softpot on the RSS screen to achieve a frequency as measured on the frequency counter to be within the limits shown in table 3-4 of the target frequency displayed on the RSS window.
6. Press Toggle PTT again to dekey the radio and then press Program to store the softpot value.

Table 3-4 Reference Oscillator Alignment.

RF-Band	Target
UHF	±150 Hz
VHF	±150 Hz

7.6 Front-End Pre-Selector

Alignment of the front-end pre-selector is normally not required on these radios. Only if the radio has poor receiver sensitivity or the pre-selector parts have been replaced the following procedure should be performed. The softpot value sets the control voltage of the pre-selector. Its value needs to be set at 7 frequencies across the frequency range.

1. Set the test box (GTF180) meter selection switch to the “Audio PA” position and connect a SINAD meter to the “METER” port.
2. From the Service menu, select Rx Alignment.
3. Select Front End Filter to open the pre-selector tuning window. The window will indicate the receive test frequencies to be used.
4. Select the first test frequency shown, and set the corresponding value to the start value shown in Table 3-5.
5. Set the RF test generator to the receive test frequency, and set the RF level to 10µV modulated with a 1kHz tone at the normal test deviation shown in table 3-6.
6. Measure the RSSI voltage at accessory connector pin 15 with a dc voltmeter capable of 1 mV resolution. The RSSI output is available on A2, 4 channel, radios but it is unbuffered. Therefore a high impedance (1 MΩ) voltmeter must be used.
7. Decrease/increase the softpot value and note the RSSI voltage. The target softpot value is achieved when the voltage change between 2 softpot steps is lower than 0.75% of the RSSI voltage for the first time. Set test box (GTF180) audio switch to the “SPKR” position. The 1kHz tone must be audible at the target value to make sure the radio is receiving.
8. Repeat steps 4 - 7 for all test frequencies shown in the window.
9. Press Program to store the softpot values.

Table 3-5 Start Value for Front-End Pre-selector Tuning.

RF-Band	Start Value
UHF VHF	Maximum Minimum

Table 3-6 Normal Test Deviation.

Channel Spacing	Deviation
12.5 kHz 20 kHz 25 kHz	1.5 kHz 2.4 kHz 3 kHz

7.7 Rated Volume

The rated volume softpot sets the volume at normal test modulation.

1. Set test box (GTF180) meter selection switch to the “AUDIO PA” position and the speaker load switch to the “MAXAR” position. Connect an AC voltmeter to the test box meter port.
2. From the Service menu, select Rx Alignment.
3. Select Rated Volume to open the rated volume tuning window. The screen will indicate the receive test frequency to be used.
4. Set the RF test generator to the receive test frequency, and set the RF level to 1mVolt modulated with a 1kHz tone at the normal test deviation shown in table 3-6. Set test box (GTF180) audio switch to the “SPKR” position. The 1kHz tone must be audible to make sure the radio is receiving.
5. Adjust the value of the softpot to obtain rated audio volume (as close to 3.74 Vrms)
   Note: The voltage at the meter port of the testbox GTF180 is only half the voltage at the speaker.
6. Press Program to store the softpot value.

7.8 Squelch

The squelch softpots set the signal to noise ratio at which the squelch opens. The squelch value needs to be set at 7 frequencies across the frequency range. For 20/25kHz radios, the radio stores separate tuning data for 20kHz and 25kHz channel spacing. Therefore, both sets of tuning data should be set independently.

1. Set the test box (GTF180) meter selection switch to the “Audio PA” position and connect a SINAD meter to the “METER” port.
2. From the Service menu, select Rx Alignment.
3. Select ‘Squelch’ to open the squelch tuning window. This window is used to set the values for 12.5kHz radios and the 25kHz data for 20/25kHz radios. The window will indicate the receive test frequencies to be used.
4. Select the first test frequency shown, and set the corresponding value to 0.
5. Set the RF test generator to the test frequency and modulate the signal generator at the normal test deviation shown in table 3-6, with 1kHz tone. Adjust the generator for a 8-10 dB SINAD level (weighted with psophometric filter).

6. Adjust the softpot value until the squelch just closes.
7. Monitor for squelch chatter; if chatter is present, repeat step 6.
8. When no chatter is detected, select the next softpot and repeat steps 4 - 7 for all test frequencies shown in the window.
9. Press Program to store the softpot values.
10. If the radio is a 20/25kHz channel spacing model, repeat steps 1-9 for 20kHz channel spacing using the 'Squelch (20kHz)' window.

7.9 Transmit Deviation Limit

The transmit deviation limit softpot sets the maximum deviation of the carrier. Unlike other radios, the deviation limit for GM350 is set using low frequency (PL) rather than the usual 1kHz tone. The deviation value needs to be set at 7 frequencies across the frequency range. No audio signals need to be injected, as the radio generates a 82.5Hz tone while the deviation limit alignment window is open. This tone is used to set the maximum deviation. For 20/25kHz radios, the radio stores separate tuning data for 20kHz and 25kHz channel spacing. Therefore, both sets of tuning data should be set independently.

1. From the Service menu, select Tx Alignment.
2. Select 'Deviation Limit' to open the deviation limit tuning window. This window is used to set the values for 12.5kHz radios and the 25kHz data for 20/25kHz radios. The window will indicate the transmit test frequencies to be used.
3. Select the first test frequency shown in the window.
4. Press Toggle PTT to key the radio. The status bar will indicate that the radio is transmitting.
5. Adjust the transmitter deviation to the value shown in table 3-7.
6. Press Toggle PTT to dekey the radio.
7. Repeat steps 3- 6 for the remaining test frequencies.
8. Press Program to store the softpot values.
9. If the radio is a 20/25kHz channel spacing model, repeat steps 1 - 8 for 20kHz channel spacing using the 'Deviation Limit (20kHz)' window.

Table 3-7 Transmitter Deviation Limit Alignment Target.

Channel Spacing	Deviation
12.5 kHz	375 Hz
20 kHz	600 Hz
25 kHz	750 Hz

7.10 Transmit Modulation Balance (Compensation)

Compensation alignment balances the modulation sensitivity of the VCO and reference modulation (synthesizer low frequency port) lines. Compensation algorithm is critical to the operation of signalling schemes that have very low frequency components (e.g. PL) and could result in distorted waveforms if improperly adjusted. The compensation value needs to be set at 7 frequencies across the frequency range. For 20/25kHz radios, the radio stores separate tuning data for 20kHz and 25kHz channel spacing. Therefore, both sets of tuning data should be set independently.

1. From the Service menu, select Tx Alignment.
2. Select 'Modulation Balance' to open the deviation balance tuning window. This window is used to set the values for 12.5kHz radios and the 25kHz data for 20/25kHz radios. The window will indicate the transmit test frequencies to be used.
3. Set the Test Box (GTF180) meter selector switch to the "GEN" position, and inject a 2kHz (two kilohertz) tone at 800 mVrms (eight-hundred millivolts) into the "Audio In" port.
4. Connect an AC meter to the meter port to insure the proper input signal level.
5. Select the first test frequency shown in the window.
6. Press Toggle PTT to key the radio. The status bar will indicate that the radio is transmitting.
7. Measure the transmitter deviation.
8. Adjust the transmitter deviation using the appropriate softpot to the value shown in Table 3-8.
9. Press Toggle PTT to dekey the radio.
10. Repeat steps 5- 9 for the remaining test frequencies.
11. Press Program to store the softpot values.
12. If the radio is a 20/25kHz channel spacing model, repeat steps 1 - 11 for 20kHz channel spacing using the 'Modulation Balance (20kHz)' window.

Table 3-8 Transmitter Deviation.

Channel Spacing	Deviation
12.5 kHz	2.1-2.2 kHz
20 kHz	3.4-3.5 kHz
25 kHz	4.3-4.5 kHz

Chapter 4

Theory of Operation

Table of Contents

Paragraph		Page
1.0	**Overview**	1
2.0	**Controller**	2
2.1	General	2
2.2	Voltage Regulators	2
2.3	Electronic On/Off	3
2.4	Mechanical On/Off	3
2.5	Ignition	3
2.6	Hook	4
2.7	Microprocessor Clock Synthesizer	4
2.8	Serial Peripheral Interface (SPI)	4
2.9	SPEB Serial Interface	5
2.10	General Purpose Input/Output	5
2.11	Normal Microprocessor Operation	5
2.12	Control Head Model A2 or A3	6
	Controller Board Audio and Signalling Circuits	
3.0	**General**	7
3.1	Audio Filter IC (AFIC)	7
3.2	Audio Ground	7
4.0	**Transmit Audio Circuits**	7
4.1	Mic Input Path	7
4.2	External Mic Path	8
4.3	PTT Sensing and TX Audio Processing	8
4.4	Option Board Audio (128ch only)	9

Paragraph Page

5.0 Transmit Signalling Circuits 10
5.1 Sub-audible Data (PL/DPL) 10
5.2 High Speed Data and DTMF 11

6.0 Receive Audio Circuits 12
6.1 Squelch Detect 12
6.2 Audio Processing and Digital Volume Control 13
6.3 Audio Amplification Speaker (+) Speaker (-) 13
6.4 Handset Audio 14
6.5 Filtered Audio 14
6.6 Discriminator Audio (Unfiltered) 14
6.7 Option Board Audio 14

7.0 Receive Signalling Circuits 15
7.1 Sub-audible Data Decoder (PL/DPL) 15
7.2 High Speed Data Decoder 15
7.3 Alert Tone Circuits 16

UHF Specific Circuit Description

8.0 Receiver Front-End 17
8.1 Front-End Band-Pass Filter & Pre-Amplifier 17
8.2 Mixer and Intermediate Frequency (IF) Section 17
8.3 IF IC (U5201) 18

9.0 Power Amplifier (PA) 5-25W. 18
9.1 Power Controlled Stage 18
9.2 PA Stages 19
9.3 Directional Coupler 19
9.4 Antenna Switch 19
9.5 Harmonic Filter 20
9.6 Power Control 20

10.0 Frequency Synthesis 21
10.1 Reference Oscillator 21
10.2 Fractional-N Synthesizer (U7501) 21
10.3 Voltage Controlled Oscillator (VCO) 22
10.4 Synthesizer Operation 22

Paragraph Page

VHF Specific Circuit Description

11.0 Receiver Front-End 24
11.1 Front-End Band-Pass Filter and Pre-Amplifier 24
11.2 Mixer and Intermediate Frequency (IF) Section 24
11.3 IF IC (U5201) 25

12.0 Power Amplifier (PA) 5-25W 25
12.1 Power Controlled Stage 25
12.2 PA Stages 26
12.3 Directional Coupler 26
12.4 Antenna Switch 26
12.5 Harmonic Filter 27
12.6 Power Control 27

13.0 Frequency Synthesis 28
13.1 Reference Oscillator 28
13.2 Fractional-N Synthesizer (U3701) 28
13.3 Voltage Controlled Oscillator (VCO) 29
13.4 Synthesizer Operation 29

1.0 Overview

This section provides a detailed theory of operation for the radio and its components.

The main radio is designed to accept one additional option board. This may provide functions such as secure voice/or a signalling decoder.

The control head is mounted directly on the front of the radio. The control head contains a speaker, LED indicators, a microphone connector, buttons and dependant of radio type, a display. These provide the user with interface control over the various features of the radio.

In addition to the power cable and antenna cable, an accessory cable can be attached to a connector on the rear of the radio. The accessory cable provides the necessary connections for items such as external speaker, foot operated PTT, ignition sensing, etc.

2.0 Controller

2.1 General

The radio controller consists of 4 main subsections:

- ☐ Digital Control
- ☐ Audio Processing
- ☐ Power Control
- ☐ Voltage Regulation

The digital control section of the radio board is based upon a closed architecture controller configuration.

The digital section consists of a microprocessor, support memory, support logic, signal MUX ICs, the On/Off circuit, and general purpose Input/Output circuitry.

The closed architecture controller uses the Motorola 68HC11E9 (U0101) for a 4 channel radio and the 68HC11E20 for a 128 channel radio. In this configuration RAM and ROM are contained within the microprocessor itself. The only external memory device in the closed architecture controller is an EEPROM (2KByte for 128 channel radio).

Note: From this point on the 68HC11E9 or E20 microprocessor will be referred to as E9/20µP or µP. References to a Control Head will be to radio model A3 (Display radio).

2.2 Voltage Regulators

Voltage regulation for the controller is provided by 3 separate devices; U0631 (LP2951CM) +5V, U0601 (LM2941T) +9.3V, and UNSW 5V (a combination of R0621 and VR0621). An additional regulator is located in the RF section.

Voltage regulation providing 5V for the digital circuitry is done by U0631. Input and output capacitors (C0631/0632 and C0633-0635) are used to reduce high frequency noise and provide proper operation during battery transients. This regulator provides a reset output (pin 5) that goes to 0 volts if the regulator output goes out of regulation. This is used to reset the controller to prevent improper operation. Diode D0631 prevents discharge of C0632 by negative spikes on the 9V3 voltage

Regulator U0601 is used to generate the 9.3 volts required by some audio circuits, the RF circuitry and power control circuitry. Input and output capacitors (C0601-0603 and C0604/0605) are used to reduce high frequency noise. R0602/R0603 sets the output voltage of the regulator. If the voltage at pin 1 is greater than 1.3 volts the regulator output decreases and if the voltage is less than 1.3 volts the regulator output increases. This regulator output is electronically disabled by a 0 volt signal on pin 2. Q0601 and associated circuitry (R0601/0604/0605 and C0606) are used to disable the regulator when the radio is turned off.

UNSW 5V is only used in a few areas which draw low current and requires 5 V while the radio is off.

UNSW 5V CL is used to buffer the internal RAM. C0622 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Diode D0621 prevents radio circuitry from discharging this capacitor.

The voltage 9V3 SUPP is only used in the VHF radio to supply the drain current for the RF MOS FET in the PA.

The voltage SW B+ is monitored by the µP through the voltage divider R0641/R0642. Diode VR0641 limits the divided voltage to 5.1V to protect the µP.

Diode D5601 (UHF) / D3601 (VHF) located on the PA section acts as protection against transients and wrong polarity of the supply voltage.

2.3 Electronic On/Off

The radio has circuitry which allows radio software and/or external triggers to turn the radio on or off without direct user action. For example, automatic turn on when ignition is sensed and off when ignition is off.

Q0611 is used to provide SW B+ to the various radio circuits. Q0611 acts as an electronic on/off switch controlled by Q0612. The switch is on when the collector of Q0612 is low. When the radio is off Q0612 is cutoff and the voltage at Q0611-base is at A+. This effectively prevents current flow through Q0611 from emitter to collector. When the radio is turned on the voltage at the base of Q0612 is high (about 0.6V) and Q0612 switches on (saturation) and pulls down the voltage at Q0611-base. With Transistor Q0611 now enabled current flows through the device. This path has a very low impedance (less than 1 ohm) from emitter to collector. This effectively provides the same voltage level at SWB+ as at A+.

The electronic on/off circuitry can be enabled by the microprocessor (through AFIC port GCB1, line B+ CONTROL), the mechanical On/Off button on the control head (line ON OFF CONTROL), or the ignition sense circuitry (line IGNITION CONTROL). If any of the 3 paths cause a low at the collector of Q0612, the electronic ON is engaged.

2.4 Mechanical On/Off

This refers to the on/off button, located on the control head, and which turns the radio on and off. If the radio is turned off and the on/off button is pressed, line ON OFF CONTROL goes high and switches the radio on as long as the button is pressed. The microprocessor is alerted through line ANALOG 3 which is pulled to low by Q0925 (Control Head Model A3) while the on/off button is pressed. If the software detects a low state it asserts B+ CONTROL via AFIC pin 39 low which keeps Q0612 and Q0611, and in turn the radio switched on.

If the on/off button is pressed and held while the radio is on, the software detects the line ANALOG 3 changing to low and switches the radio off by setting B+ CONTROL to low.

2.5 Ignition

Ignition sense is used to prevent the radio from draining the vehicle's battery because the engine is not running.

When the IGNITION input (J0400- 10) goes above 6 volts Q0421 and Q0612 turn on. This turns on SW B+ by turning on Q0611 via line IGNITION CONTROL and Q0612 and the microprocessor starts execution. The software reads the line IGNITION SENSE, determines from the level that the IGNITION input is active and sets the B+ CONTROL output of the AFIC pin 39 to high to latch on SW B+.

When the IGNITION input goes below 6 volts, Q0421 switches off and R0426, R0427 pull line IGNITION SENSE high. The software is alerted by line IGNITION SENSE to switch off the radio by setting B+ CONTROL to low. The next time the IGNITION input goes above 6 volts the above process will be repeated.

2.6 Hook

The HOOK input is used to inform the µP when the Microphone´s hang-up switch is engaged. The signal is routed from J0101-3 and transistor Q0137 to the E9/20µP U0101-56. The voltage range of HOOK in normal operating mode is 0-5V. If a rear GP input line is set as HOOK then the front HOOK signal is overriden.

2.7 Microprocessor Clock Synthesizer

The controller uses the oscillator in the microprocessor E9/20µP along with some external components (C0115-C0117, L0114, R0115, Y0114) to generate the clock. Q0114 is used to alter the clock frequency slightly under software control if there is a possibility of harmonics of this clock source interfering with the desired radio receive frequency.

2.8 Serial Peripheral Interface (SPI)

The µP communicates to many of the IC's through its SPI port. This port consists of SPI TRANSMIT DATA (MOSI) (E9/20µP:U0101-52), SPI RECEIVE DATA (MISO) (E9/20µP:U0101-51), SPI CLK (E9/20µP:U0101-53) and chip select lines going to the various IC's, connected on the SPI PORT (BUS). This BUS is a synchronous bus, in that the timing clock signal CLK is sent while SPI data (SPI TRANSMIT DATA or SPI RECEIVE DATA) is sent. Therefore, whenever there is activity on either SPI TRANSMIT DATA or SPI RECEIVE DATA there should be a uniform signal on CLK. The SPI TRANSMIT DATA is used to send serial from a µP to a device, and SPI RECEIVE DATA is used to send data from a device to a µP. The only device from which data can be received via SPI RECEIVE DATA is the EEPROM (U0108)

On the controller there are three ICs on the SPI BUS, AFIC (U103-33), EEPROM (U0108-1) and D/A (U0731-6). In the RF sections there is one IC on the SPI BUS, the FRAC-N Synthesizer. The SPI TRANSMIT DATA and CLK lines going to the RF section are filtered by L0194/L0195 to minimize noise. The chip select lines for the IC´s are decoded by the address decoder U102.

The SPI BUS is also used for the control head. U0104-1,2 buffer the SPI TRANSMIT DATA and CLK lines to the control head. U0104-3 switches off the CLK signal for the LCD display if it is not selected via LCD CE.

When the µP needs to program any of these IC's it brings the chip select line for that IC to a logic 0 and then sends the proper data and clock signals. The amount of data sent to the various IC's are different, for example the FRAC-N can receive up to 13 bytes (97 bits) while the DAC can receive up to 3 bytes (24 bits). After the data has been sent the chip select line is returned to a logic 1.

The Option board interfaces are different in that the µP can also read data back from devices connected.

The timing and operation of this interface is specific to the option connected, but generally follows the pattern:

1) an option board device generates the interrupt,
2) main board asserts a chip select for that option board device,
3) the main board μP generates the CLK, and
4) when data transfer is complete the main board terminates the chip select and CLK activity.

2.9 SPEB Serial Interface

The SBEP serial interface allows the radio to communicate with the Radio Service Software (RSS). This interface connects to the Microphone connector (J0903/J0803) via Control Head connector (J0101) and comprises BUS+ (J0101-15). The line is bi-directional, meaning that either the radio or the RSS can drive the line.

When the RSS needs to communicate with the radio, an interrupt is generated by the BUS+ signal through R0104. The μP then starts serial data communication on BUS+ by sending data from pin 50 through D0101 and receiving data at pin 47 through R0104. While the radio is sending serial data at pin 50 it receives an ”echo” of the same data at pin 47.

2.10 General Purpose Input/Output

The Controller provides six general purpose lines (GP1 through GP6) available on the accessory connector J0400 to interface to external options. Lines GP1,4 are inputs, GP2 is an output and GP3,5,6 are bidirectional. The software and the hardware configuration of the radio model define the function of each port. Some ports are not connected on the 4ch radio, refer to appendix B.

GP1 can be used as external PTT input or others, set by the RSS.

GP2 can be used as normal output (Q0441 placed) or external alarm output (Q0442 placed). The voltage range can be set by R0442 (0-5V) or R0443 (0 - supply voltage).

GP4 can be used as normal input (D0471, R0477 not placed) or emergency input (D0471, R0477 placed).

GP3,5,6 are bidirectional and use the same circuit configuration. Each port uses an output transistor controlled by μP port PB5,4,7 and an input transistor read by μP port PC2,5,3. To use one of the GP´s as input the μP must turn off the corresponding output transistor.

In addition the signals from GP3-6 are fed to the option board connectors J0102, J0103.

The 470pF and 10nF capacitors serve to filter out any AC noise which may ride on the GP lines.

2.11 Normal Microprocessor Operation

The E9/20μP (U0101) contains internal 12 (E9) or 20 (E20) Kilobytes ROM, 512 (E9) or 768 (E20) bytes SRAM and 512 bytes EEPROM.

The E9/20μP RAM is always powered to maintain parameters such as the last operating mode. This is achieved by maintaining 5V at U0101-25. Under normal conditions, when the radio is off UNSW +5V is formed by FLT A+ running to D0621.

C0622 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Diode D0621 prevents radio circuitry from discharging this capacitor.

U0101-22 is the high reference voltage for the A/D ports on the E9/20µP. Resistor R0105 and capacitor C0105 filter the +5V reference. If this voltage is lower than +5V the A/D readings will be incorrect. Likewise U0101-21 is the low reference for the A/D ports. This line is normally tied to ground. If this line is not connected to ground, the A/D readings will be incorrect.

The MODB (U0101-25) input of the E9/20µP must be at a logic 1 for it to start executing correctly. The XIRQ (U0101-45) and the IRQ (U0101-46) pins should also be at a logic 1.

Optional external EEPROM (U0108) is available on some radio models. The external EEPROM is accessed through a serial connection. The E9/20µP generates SPI CLK (U0101-53), SPI TRANSMIT DATA (MOSI) (U0101-52) and SPI RECEIVE DATA (MISO) (U0101-51) to read or write EEPROM. On a read of EEPROM the E9/20µP continues generating the clock and the EEPROM places the requested data on the SPI RECEIVE DATA (MISO) line. On a write the message is followed by the data to be written to the EEPROM.

2.12 Control Head Model A2 or A3

Two Control Head versions (A2 or A3) are available for user interface. Both Control Heads contain the internal speaker, the microphone connector, several buttons to operate the radio and several indicator LEDs to inform the user about the radio status. Additionally the Control Head model A3 uses a 3 digit, 7 segment, LCD display for the channel number.

The On/Off button when pressed switches the voltage regulators on by pulling ON OFF CONTROL to high and connects the base of Q0925(A3), Q0825(A2) to FLT A+. This transistor pulls the line ANALOG 3 to low to inform the µP that the On/Off button is pressed. If the radio is switched off, the µP will switch it on and vice versa. All other buttons work the same way. If a button is pressed, it will connect one of the 3 lines ANALOG 1,2,3 to a resistive voltage divider connected to +5V. The voltages of the lines are A/D converted inside the µP and specify the pressed button.

All the back light and indicator LEDs are driven by current sources and controlled by the µP via SERIAL PERIPHERAL INTERFACE (SPI) interface. The LED status is stored in shiftregister U0941(A3), U0841(A2). Line LED CE enables the serial write process via Q0941(A3), Q0841(A2) while line LED CLCK BUF shifts the data of line SPI DATA BUF into the shiftregister.

In addition Control Head Model A3 contains the LCD display H0931. The display data of line SPI DATA BUF is shifted into the display driver by clock signal LCD CLCK BUF.

CONTROLLER BOARD AUDIO AND SIGNALLING CIRCUITS

3.0 General

3.1 Audio Filter IC (AFIC)

The AFIC (U0103) used in the controller performs RX/TX audio shaping, i.e. filtering, amplification, attenuation.

The AFIC is programmable through the SPI BUS (U0103-30/31/33), normally receiving 6 bytes. This programming sets up various paths within the AFIC to route audio signals through the appropriate filtering, gain and attenuator blocks. The AFIC also has 4 General Control Bits GCB1,3-5 which are CMOS level outputs. GCB1 is used to switch the radio on and off under µP control via line B+ CONTROL. GCB3 is used to switch the audio PA on and off (AUDIO PA ENABLE). GCB4 selects between the UNATTEN RX OUT audio signal and the unfiltered DET AUDIO signal. GCB5 HIGH LOW BAND can be used to switch between band splits.

3.2 Audio Ground

VAG is the dc bias used as an audio ground for the op-amps that are external to the Audio Filter IC (AFIC). U0105-1 forms this bias by dividing 9.3V with resistors R0171, R0172 and buffering the 4.65V result with a voltage follower. VAG emerges at pin 1 of U0105-1. C0172 is a bypass capacitor for VAG. The AFIC generates its own 2.5 V bias for its internal circuitry. C0153 is the bypass for the AFIC's audio ground dc bias. Note that while there are AFIC VAG, and BOARD VAG (U0105-1) each of these are separate. They do not connect together.

4.0 Transmit Audio Circuits

Refer to Figure 4-1 for reference for the following sections.

4.1 Mic Input Path

The radio supports 2 distinct microphone paths known as internal and external mic and an auxiliary path (FLAT TX AUDIO). The microphones used for the radio require a DC biasing voltage provided by a resistive network.

These two microphone audio inputs are connected together. Following the internal mic path; the microphone is plugged into the radio control head and is connected to the controller board via J0101-16. From here the signal is routed to C0142. R0141 and R0142 provide the 9.3VDC bias. R0142 and C0141 provide a 1kΩ AC path to ground that sets the input impedance for the microphone and determines the gain based on the emitter resistor in the microphone's amplifier circuit.

The MIC signal is routed to the AFIC´s TX IN input (U0103-10) through R0146 and R0145 (4 channel radio) or through op-amp buffer U0106-2 and option board connector J0103-3,1 (128 channel radio). The audio signal at the output of U0106-2 should be approximately 80mV deviation with 25kHz channel spacing.

The FLAT TX AUDIO signal from accessory connector U0400-5 is buffered by op-amp U0106-1 and fed to the AFIC U0103-13 through gate U0107-1. Gate U0107-1 is controlled by the μP port PC7 (U0101-42) and selects between FLAT TX AUDIO or signalling signal created by the μP.

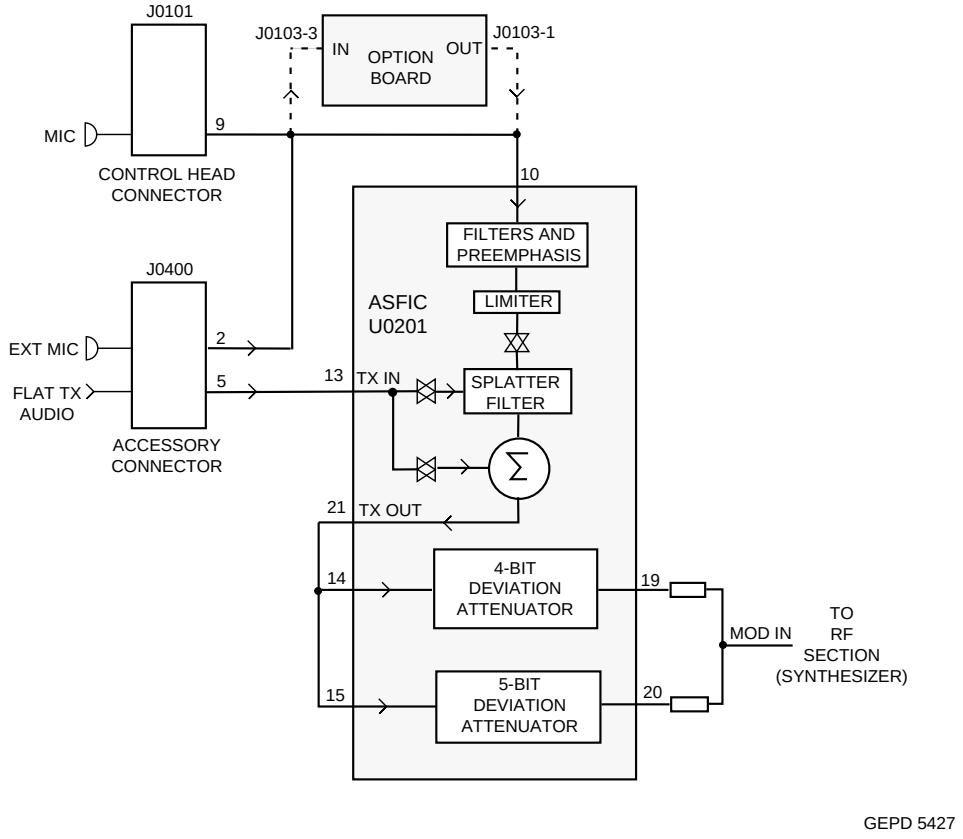


Figure 4-1 Transmit Audio Paths

4.2 External Mic Path

The external microphone signal enters the radio on accessory connector J0400 pin 2 and connects to the standard microphone input through R0421.

4.3 PTT Sensing and TX Audio Processing

Mic PTT is sensed by the μP U0101 pin 22. An external PTT can be generated by grounding pin 3 on the accessory connector if this input is programmed for PTT.

The MIC signal is routed to the AFIC (U0103) through R0146 and R0145 (4 channel radio) or through op-amp buffer U0106-2 and option board connector J0103-3,1 (128 channel radio). R0145, C0145, the amplifier inside the AFIC (pins 9,10) and gain setting resistor R0147 pre-emphasise the MIC audio signal. After further limiting and filtering the modulation signal emerges from the AFIC at U0103-19/20. Both signals are weighted by resistors R0181, R0182 and add up to signal MOD IN.

4.4 Option Board Audio (128ch only)

The audio coming from the microphone (J0101-16) or the external microphone (J0400-2) is routed through op-amp buffer U0106-2 (128ch only) to the option board connector J0103-3. After option board processing the signal emerges at J0103-1. The source resistor of the option board output and C0145, the amplifier inside the AFIC (U0103-9,10) and gain setting resistor R0147 pre-emphasise the signal. Inside the AFIC the signal follows a path identical to conventional transmit audio. The modulation signal emerges from the AFIC at J0103-19/20. Both signals are weighted by resistors R0181, R0182 and add up to signal MOD IN.

5.0 Transmit Signalling Circuits

Refer to Figure 4-2 for reference for the following sections. From a hardware point of view, there are three types of signalling:

1. Sub-audible data (PL / DPL / Connect Tone) that gets summed with transmit voice or signalling,
2. DTMF data for telephone communication in trunked and conventional systems, and
3. Audible signalling including Select 5, MPT-1327, MDC, Single Tones.

All three types are supported by the hardware while the radio software determines which signalling type is available. Currently only PL/DPL and Single tones are supported in the software.

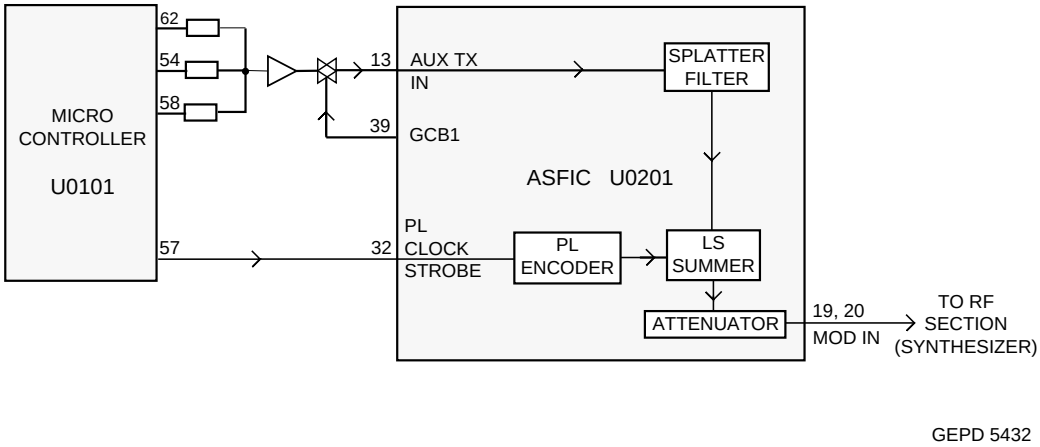


Figure 4-2 Transmit Signalling Paths

5.1 Sub-audible Data (PL/DPL)

Sub-audible data implies signalling whose frequency is below 300Hz. Although it is referred to as ”sub-audible data,” the actual frequency spectrum of these waveforms may be as high as 250 Hz, which is audible to the human ear. However, the radio receiver filters out any audio below 300Hz, so these tones are never heard in the actual system.

Only one type of sub-audible data can be generated by U0103 (AFIC) at any one time. The process is as follows, using the SPI BUS, the μP programs the AFIC to set up the proper low-speed data deviation and select the PL or DPL filters. The μP then generates a square wave which strobes the AFIC PL / DPL encode input PL CLOCK STROBE U0103-32 at twelve times the desired data rate. For example, for a PL frequency of 103Hz, the frequency of the square wave would be 1236Hz.

This drives a tone generator inside U0103 which generates a staircase approximation to a PL sine wave or DPL data pattern. This internal waveform is then low-pass filtered and summed with voice or data. The resulting summed waveform then appears on U0103-19,20 (MOD IN), where it is sent to the RF board as previously described for transmit audio.

5.2 High Speed Data and DTMF

The High Speed Data and DTMF waveforms are created by the μP U0101 using summer U0105-3. Op-amp U0105-3 and resistors R0121-R0124 add up the three signals coming from the μP pins 58, 59 and 62. The output signal of U0105-3 is routed to the AFIC (U0103-13) through gate U0107-1. Inside the AFIC the signal enters the conventional transmitter audio path at the splatter filter input. Gate U0107-1 controlled by μP port PC7 (U0101-42) selects between data signal and FLAT TX AUDIO signal. Microphone audio is muted during High Speed Data signalling.

6.0 Receive Audio Circuits

Refer to Figure 4-3 for reference for the following sections.

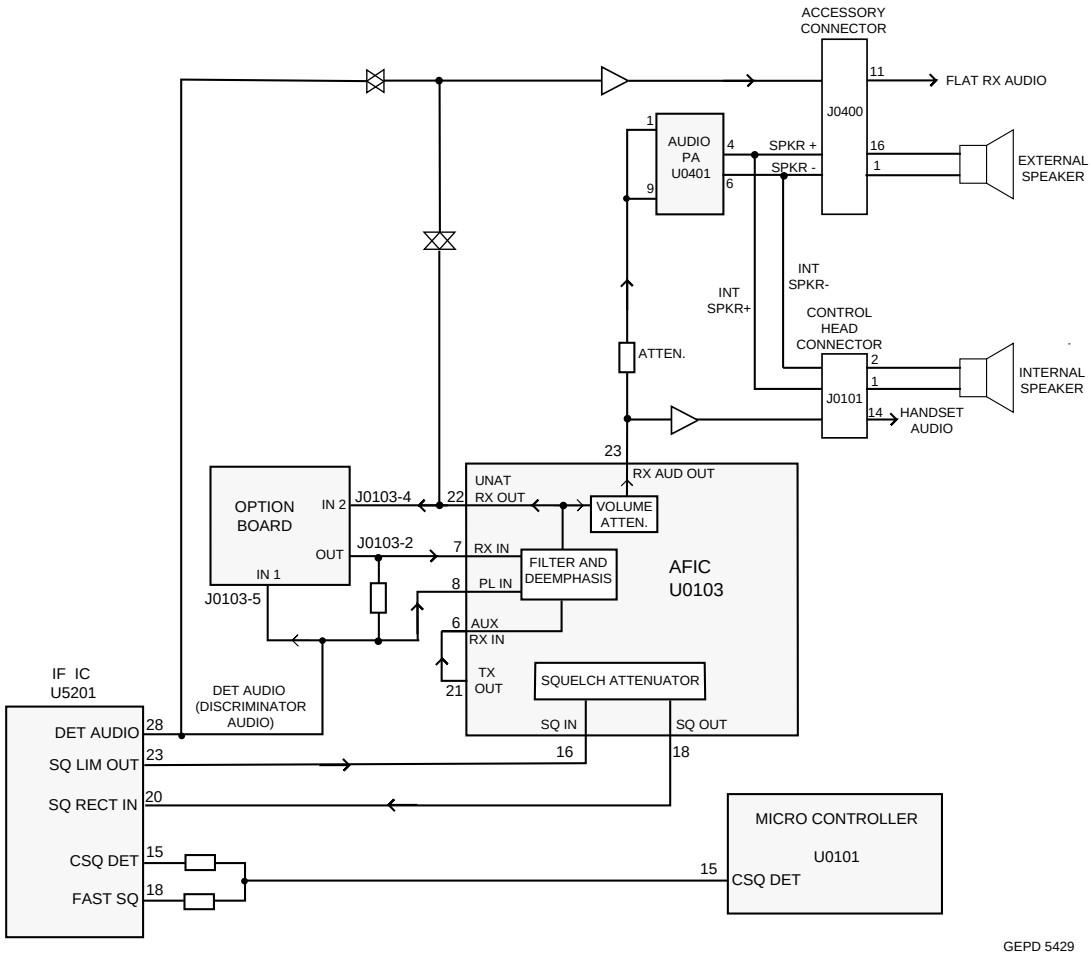


Figure 4-3 Receive Audio Paths.

6.1 Squelch Detect

The IF IC controls the squelch characteristics of the radio. With a few external parts (R5222, C5229, C5230, R5223) the squelch tail, hysteresis, attack and delay are optimized for the radio. To set the squelch threshold the signal from IF IC pin 23 (line SQ ATT IN) is routed to the squelch attenuator input of the AFIC (U0103-16). The attenuated signal (line SQ ATT OUT) from the AFIC (U0103-18) enters the IF IC at pin 20 and is used to create a squelch indicator signal available at pin 15 (line CSQ DET).

The microprocessor controlled ADAPT signal at pin 22 activates the fast squelch indicator signal at IF IC pin 18 (FAST SQ). Both squelch indicator signals CSQ DET (pin 15) and FAST SQ (pin 18) are combined, weighted by resistors R0111 / R012 and fed to one of the microprocessor´s ADCs (U0101-15) for interpretation. From the voltage weighted by the resistors the µP determines whether CSQ DET, FAST SQ or both are active.

6.2 Audio Processing and Digital Volume Control

The receiver audio signal enters the controller section from the IF IC (U5201-28) on DET AUDIO. The signal is AC coupled by C0181 and enters the AFIC via the RX IN pin U0103-7.

Inside the AFIC the signal entering RX IN (U0103-7) goes through the audio path while the signal entering PL DPL IN (U0103-8) via C0182 goes through the PL/DPL path.

The audio path has a programmable amplifier, whose setting is based on the channel bandwidth being received, then a LPF filter to remove any frequency components above 3000Hz and then an HPF to remove any sub-audible data below 300Hz. Next, the recovered audio passes through a de-emphasis filter if it is enabled (to compensate for Pre-emphasis which is used to reduce the effects of FM noise). The IC then passes the audio through the 8-bit programmable attenuator whose level is set depending on the value of the volume control. Finally, the filtered audio signal passes through an output buffer within the AFIC. The audio signal exits the AFIC at RX AUDIO U0103-23.

The µP programs the attenuator, using the SPI BUS, based on the volume setting. The minimum/ maximum settings of the attenuator are set by codeplug parameters.

Since sub-audible signalling is summed with voice information on transmit, it must be separated from the voice information before processing. Any sub-audible signalling enters the AFIC from the IF IC at PL DPL IN U0103-8. Once inside it goes through the PL/DPL path. The signal first passes through one of 2 low pass filters, either PL low pass filter or DPL/LST low pass filter. Either signal is then filtered and goes through a limiter and exits the AFIC at PL DPL DECODER OUT U0103-27. At this point the signal will appear as a square wave version of the sub-audible signal which the radio received. The microprocessor (U0101-64) will decode the signal directly to determine if it is the tone/ code which is currently active on that mode.

6.3 Audio Amplification Speaker (+) Speaker (-)

The output of the AFIC´s digital volume pot, U0103-23 is routed through a voltage divider formed by R0401 and R0402 to set the correct input level to the audio PA (U0401). This is necessary because the gain of the audio PA is 46 dB, and the AFIC output is capable of overdriving the PA unless the maximum volume is limited.

The audio then passes through C0401 which provides AC coupling and low frequency roll-off. C0402 provides high frequency roll-off as the audio signal is routed to pins 1 and 9 of the audio power amplifier U0401.

The audio power amplifier has one inverted and one non-inverted output that produces the differential audio output SPK+ / SPK- (U0401-4/6). The inputs for each of these amplifiers are pins 1 and 9 respectively; these inputs are both tied to the received audio. The audio PA's DC biases are not activated until the audio PA is enabled at pin 8.

The audio PA is enabled via AUDIO PA ENABLE signal from the AFIC (U0103-40). When the base of Q0401 is low, the transistor is off and U0401-8 is high, using pull up resistor R0406, and the Audio PA is ON. The voltage at U0401-8 must be above 8.5VDC to properly enable the device. If the voltage is between 3.3 and 6.4V, the device will be active but has its input (U0401-1/9) off. R0404 ensures that the base of Q0401 is high on power up. Otherwise there may be an audio pop due to R0406 pulling U0401-8 high before the software can switch on Q0401.

The SPK+ and SPK- outputs of the audio PA have a DC bias which varies proportionately with FLT A+ (U0401-7). FLT A+ of 11V yields DC offset of 5V, and FLT A+ of 17V yields a DC offset of 8.5V. If either of these lines is shorted to ground, it is possible that the audio PA will be damaged. SPK+ and SPK- are routed to the accessory connector (J400-16 and 1) and to the control head (connector J0101-1 and 2).

6.4 Handset Audio

Certain hand held accessories have a speaker within them which require a different voltage level than that provided by U0401. For those devices HANDSET AUDIO is available at J0101-14.

The received audio from the output of the AFIC´s digital volume attenuator is also routed to U0105-4 pin 9 where it is amplified 15 dB; this is set by the 10k/68k combination of R0154 and R0155. This signal is routed from the output of the op amp U0105-4 pin 8 to J0101-14. The control head sends this signal directly out to the microphone jack. The maximum value of this output is 6.6Vp-p.

6.5 Filtered Audio

The AFIC has an audio whose output at U0103-22 has been filtered and de-emphasized, but has not gone through the digital volume attenuator. From AFIC U0103-22 the signal is routed through gate U0107-2 and AC coupled to U0106-4. The gate controlled by AFIC port GCB4 (U0103-2) selects between the filtered audio signal from the AFIC or the unfiltered discriminator signal from the IF IC U5201.The output at U0106-4 is then routed to J0400-11. Note that any volume adjustment of the signal on this path must be done by the accessory.

6.6 Discriminator Audio (Unfiltered)

Note that discriminator audio DET AUDIO from the IF IC U5201, in addition to being routed to the AFIC, is also routed to the option connector J0103-5 (See Secure Rx description blocks for further information).

6.7 Option Board Audio

Discriminator or filtered audio, enters the option board at connector J0103-5 and J0103-4. On the option board, the signal may be processed and then fed back through (J0103-2) to AUX RX IN of the AFIC (U0103-6). From then on it follows a path identical to conventional receive audio, where it is filtered (0.3 - 3kHz) and de-emphasized.

7.0 Receive Signalling Circuits

Refer to Figure 4-4 for reference for the following sections.

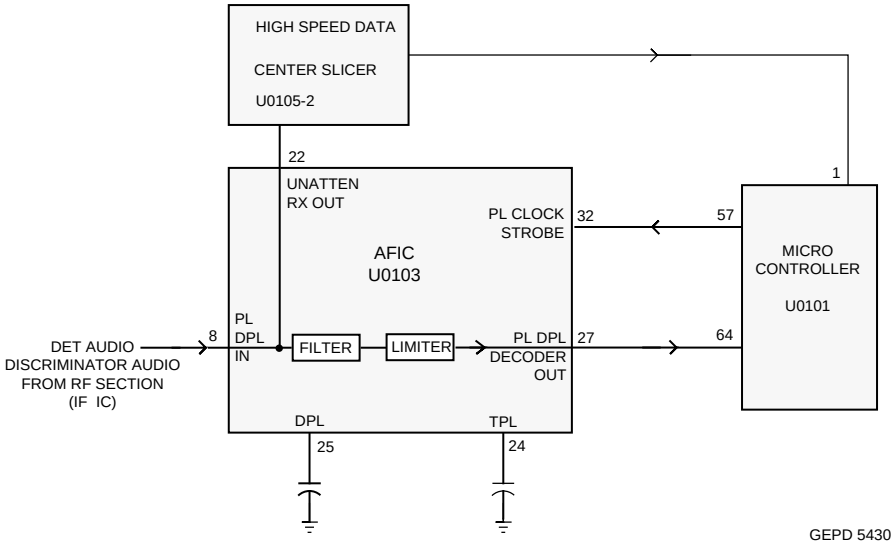


Figure 4-4 Receive Signalling Path.

7.1 Sub-audible Data Decoder (PL/DPL)

The receiver audio signal entering the AFIC U0103 at pin 8 first passes through the Tone PL filter or the Digital PL filter, depending on the PL option selected for the current operating mode. Filtered PL is then coupled to the PL detector circuit, with detected PL output at U0103-27. At this point the signal will appear as a square wave version of the sub-audible signal which the radio received. The microprocessor U0101-64 will decode the signal directly to determine if it is the tone / code which is currently active on that mode.

7.2 High Speed Data Decoder

The unattenuated receiver audio signal from U0103-22 is AC coupled to the input of centre slicer circuit U0105-2. The non-inverting input of op-amp U0105-2 is fed through resistor R0162. Capacitor C0164 sets a low-pass corner frequency of 3.3kHz. The inverting input of op-amp U0105-2 is fed through resistor R0163. Capacitor C0163 sets a low-pass corner frequency of 16Hz.

During operation, R0163 / C0163 establish an average DC offset level at U0105-2 pin 6 dependent on the average DC level of the undetected signal to set the “trigger” threshold of U0105-2. R0162 / C0164 provide high audio frequency roll-off to improve falsing immunity, but passes 600 or 1200 baud signals. The detected output from the centre slicer circuit is buffered and inverted by Q0161 and then coupled to the µP U0101-1 where algorithms perform the final decoding.

7.3 Alert Tone Circuits

When the software determines that it needs to give the operator an audible feedback (for a good key press, or for a bad key press), or radio status , it sends an alert tone to the speaker.

It does so by sending SPI BUS data to U0103 which sets up the audio path to the speaker for alert tones. The alert tone itself is generated by the AFIC.

The allowable internal alert tones are 410, 820, and 1640Hz. In this case a code contained within the SPI BUS load to the AFIC sets up the path and determines the tone frequency, and at what volume level to generate the tone. (It does not have to be related to the voice volume setting).

Inside the AFIC, this signal is routed to the alert tone generator; the output of the generator is summed into the audio chain just after the RX audio de-emphasis block. Inside U0103 the tone is amplified and filtered, then passed through the 8-bit digital volume attenuator, which is typically loaded with a special value for alert tone audio. The tone exits at U0103-23 and is routed to the audio PA like receive audio.

UHF SPECIFIC CIRCUIT DESCRIPTION

8.0 Receiver Front-End

The receiver is able to cover the UHF range from 403 to 470 MHz. It consists of four major blocks: front-end, mixer, first IF section and IF IC. Antenna signal pre-selection is performed by two varactor tuned bandpass filters. A double balanced shottky diode mixer converts the signal to the first IF at 45.1 MHz.

Two crystal filters in the first IF section and two ceramic filters in the second IF section provide the required selectivity. The second IF at 455 kHz is mixed, amplified and demodulated in the IF IC. The processing of the demodulated audio signal is performed by an audio processing IC located in the controller section.

8.1 Front-End Band-Pass Filter & Pre-Amplifier

A two pole pre-selector filter tuned by the varactor diodes D5301 and D5302 pre-selects the incoming signal (PA RX) from the antenna switch to reduce spurious effects to following stages. The tuning voltage (FE CNTL VLTG) ranging from 2 volts to 8 volts is controlled by a Digital to Analog (D/A) converter (U0731-11) in the controller section. A dual hot carrier diode (D5303) limits any inband signal to 0 dBm to prevent damage to the pre-amplifier.

The RF pre-amplifier is an SMD device (Q5301) with collector base feedback to stabilize gain, impedance, and intermodulation. The collector current of approximately 11-16 mA is drawn from the voltage 9V3.

A second two pole varactor tuned bandpass filter provides additional filtering to the amplified signal. The varactor diodes D5304 and D5305 are controlled by the same signal which controls the pre-selector filter. A following 3 dB pad (R5310, R5314, R5316) stabilizes the output impedance and intermodulation performance.

If the UHF radio is configured for a base station application, R5319 is not placed and TP5301 and TP5302 are shorted.

8.2 Mixer and Intermediate Frequency (IF) Section

The signal coming from the front-end is converted to the first IF (45.1 MHz) using a double balanced schottky diode mixer (D5401). Its ports are matched for incoming UHF signal conversion to the 45.1MHz IF using low side injection. The injection signal (VCO MIXER) coming from the mixer buffer (Q5771) is filtered by the lowpass consisting of (L5403, L5404, C5401 - C5403) and has a level of approximately 10 dBm.

The mixer IF output signal (RX IF) from transformer T5401 pin 2 is fed to the first two pole crystal filter Y5201. The filter output in turn is matched to the following IF amplifier.

The IF amplifier Q5201 is actively biased by a collector base feedback (R5201, R5202) to a current drain of approximately 5 mA drawn from the voltage 5V STAB. Its output impedance is matched to the second two pole crystal filter Y5202. A dual hot carrier diode (D5201) limits the filter output voltage swing to reduce overdrive effects at RF input levels above -27 dBm.

8.3 IF IC (U5201)

The first IF signal from the crystal filters feeds the IF IC (U5201) at pin 6. Within the IF IC the 45.1MHz first IF signal mixes with the second local oscillator (LO) at 44.645MHz to the second IF at 455 kHz. The second LO uses the external crystal Y5211. The second IF signal is amplified and filtered by two external ceramic filters (FL5201, FL5202). Back in the IF IC the signal is demodulated in a phase-lock detector and fed from IF IC pin 28 to the audio processing circuit AFIC U0103 located in the controller section (line DET AUDIO).

The IF IC also controls the squelch characteristics of the radio. With a few external parts (R5222, C5229, C5230, R5223) the squelch tail, hysteresis, attack and delay were optimized for the radio. To set the squelch threshold the signal from IF IC pin 23 (line SQ ATT IN) is attenuated by a microprocessor controlled audio processing IC AFIC (U0103) located in the controller section. The attenuated signal from the AFIC (line SQ ATT OUT) enters the IF IC at pin 20 and is used to create a squelch indicator signal available at pin 15 (CSQ DET).

The microprocessor controlled ADAPT signal at pin 22 activates the fast squelch indicator signal at IF IC pin 18 (FAST SQ). Both squelch indicator signals CSQ DET (pin 15) and FAST SQ (pin 18) are combined, weighted by R0111 / R0112 and fed to the microprocessor U0101 pin 15 for interpretation. From the voltage weighted by the resistors the µP determines whether CSQ DET, FAST SQ or both are active.

At IF IC pin 11 an RSSI signal is available with a dynamic range of 70 dB. The RSSI signal is buffered by op-amp U0106-3 and available at accessory connector J0400-15.

9.0 Power Amplifier (PA) 5-25W.

The radio's 5-25 W PA is a four stage amplifier used to amplify the output from the exciter to the radio transmit level. It consists of four stages in the line-up. The first (Q5510) is a bipolar stage that is controlled via the PA control line. It is followed by another bipolar stage (Q5520), a MOS FET stage (Q5530) and a final bipolar stage (Q5536).

Devices Q5510 and Q5520 are surface mounted. MOS FET Q5530 and bipolar Transistor Q5536 are directly attached to the heat sink.

9.1 Power Controlled Stage

The first stage (Q5510) amplifies the RF signal from the VCO (line EXCITER PA) and controls the output power of the PA. The output power of the transistor Q5510 is proportional to its collector current which is adjusted by a voltage controlled current source consisting of Q5612 and Q5621. The whole stage operates off the K9V1 source which is 9.1V in transmit mode and nearly 0V in receive mode.

The collector current of Q5510 causes a voltage drop across the resistors R5623 and R5624. Transistor Q5612 adjusts the voltage drop across R5621 through PA control line (PWR CNTL). The current source Q5621 adjusts the collector current of Q5510 by modifying its base voltage until the voltage drop across R5623 and R5624 plus VBE (0.6V) equals the voltage drop across R5621 plus VBE (0.6V) of Q5611. If the voltage of PWR CNTL is raised, the base voltage of Q5612 will also rise causing more current to flow to the collector of Q5612 and a higher voltage drop across R5621. This in turn results in more current driven into the base of Q5510 by Q5621 so that the current of Q5510 is increased. The collector current settles when the voltage over the series configuration of R5623 and R5624 plus VBE of Q5621 equals the voltage over R5621 plus VBE (0.6V) of Q5611.

By controlling the output power of Q5510 and in turn the input power of the following stages the ALC loop is able to regulate the output power of the transmitter.

9.2 PA Stages

The bipolar transistor Q5520 is driven by Q5510. To reduce the collector - emitter voltage and in turn the power dissipation of Q5510 its collector current is drawn from the antenna switch circuit.

In transmit mode the base of Q5520 is slightly positive biased by a divided K9V1 signal to allow a collector current to be drawn from the antenna switch circuit and in turn switches the antenna switch to transmit while in receive mode the low K9V1 signal cuts off the collector current and in turn switches the antenna switch to receive.

The following stage uses an enhancement mode N-Channel MOS FET device (Q5530) and requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line BIAS VLTG is set in transmit mode by a Digital to Analog (D/A) converter (U0731-4) and fed to the gate of Q5530 via a resistive divider. The bias voltage is tuned in the factory. If the transistor is replaced, the bias voltage must be tuned with the Radio Service Software (RSS). Care must be taken, not to damage the device by exceeding the maximum allowed bias voltage. The collector current is drawn from the supply voltage A+.

The final stage uses the bipolar device Q5536 and operates off the A+ supply voltage. For class C operation the base is DC grounded by two series inductors (L5533, L5534). A matching network consisting of C5542-C5544 and two striplines transform the impedance to 50 Ohms and feed the directional coupler.

9.3 Directional Coupler

The directional coupler is a microstrip printed circuit which couples a small amount of the forward power off the RF power from Q5536. The coupled signal is rectified to an output power proportional negative DC voltage by the diode D5553 and sent to the power control circuit in the controller section via the line PWR DETECT for output power control. The power control circuit holds this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

9.4 Antenna Switch

The antenna switch is switched synchronously with the K9V1 voltage and feeds either the antenna signal coming through the harmonic filter to the receiver or the transmitter signal coming from the PA to the antenna via the harmonic filter.

In transmit mode, this K9V1 voltage is high and biases Q5520 to allow a collector current to be drawn. The collector current of Q5520 drawn from A+ flows via L5542,L5541, directional coupler, D5551, L5551, D5631, L5631, R5616, R5617 and L5611 and switches the PIN diodes D5551 and D5631 to the low impedance state. D5551 leads the RF signal from the directional coupler to the harmonic filter. The low impedance of D5631 is transformed to a high impedance at the input of the harmonic filter by the resonant circuit formed by L5551,C5633 and the input capacitance of the harmonic filter.

In receive mode the low K9V1 turns off the current through the PIN diodes and switches them to the high impedance state. The antenna signal, coming through the harmonic filter, is channelled to the receiver via L5551, C5634 and line PA RX.

A high impedance resonant circuit formed by D5551 in off state and L5554, C5559 prevents an influence of the receive signal by the PA stages. The high impedance of D5631 in off state doesn´t influence the receiver signal.

9.5 Harmonic Filter

The transmitter signal from the antenna switch is channelled through the harmonic filter to the antenna connector J5501.The harmonic filter is formed by inductors L5552, L5553, and capacitors C5557,C5552 through C5555. This network forms a low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R5550 is used for electro - static protection.

9.6 Power Control

The power control loop regulates transmitter power with an automatic level control (ALC) loop and provides protection features against excessive control voltage and high operating temperatures.

MOS FET device bias, power and control voltage limit are adjusted under microprocessor control using a Digital to Analog (D/A) converter (U0731). The microprocessor writes the data into the D/A converter via serial interface (SRL) composed of the lines SPI CLCK SRC (clock), SPI DATA SRC (data) and DAC CE (chip enable). The D/A adjustable control voltage limit increases transmitter rise time and reduces adjacent channel splatter as it is adjusted closer to the actual operating control voltage.

The microprocessor controls K9V1 ENABLE (U0101-6) to switch on the first and the second PA stage via K9V1. The antenna switch is turned on by the collector current of the second PA stage. PA DISABLE, also microprocessor controlled (U0101-54), sets BIAS VLTG (U0731-4) and VLTG LIMIT SET (U0731-13) in receive mode to low to switch off the bias of the MOS FET device Q5530 and to switch off the power control voltage (PWR CNTL).

Through an Analog to Digital (A/D) input (VLTG LIMIT) the microprocessor can read the PA control voltage (PWR CNTL) during the tuning process.

The ALC loop regulates power by adjusting the PA control line PWR CNTL to keep the forward power voltage PWR DETECT at a constant level.

Opamp U0701-2 and resistors R0701 to R0703 and R0731 subtract the negative PWR DETECT voltage from the PWR SET D/A output U0731 pin 2. The result is connected to opamp inverting input U0701-4 pin 9. This voltage which is compared with a 4.6 volt reference VAG present at noninverting input U0701-4 pin 10 and controls the output power of the PA via pin 8 and control line PWR CNTL. The 4.6 volt reference VAG is set by a resistive divider circuit (R0171, R0172) which is connected to ground and 9.3 volts and buffered by opamp U0105-1.

During normal transmitter operation the voltages at the opamp inputs U0701-4 pins 9 and 10 should be equal to 4.6 volts and the PA control voltage output at pin 8 should be between 4 and 7 volts. If power falls below the desired setting, PWR DETECT increases, causing the output at U0701-2 pin 7 to decrease and the opamp output U0701-4 pin 8 to increase.

A comparator formed by U0701-4 increases the PA control voltage PA CNTL until PWR DETECT is at the desired level. The power set D/A output voltage PWR SET (U0731-2) at U0701-2 pin 5 adjusts power in steps by adjusting the required value of PWR DETECT. As PWR SET (U0731-2) decreases, transmitter power must increase to make PWR DETECT larger and keep the inverting input U0701-4 pin 9 at 4.6 volts.

Loop frequency response is controlled by opamp feedback components R0712 and C0711. Opamp U0701-3 compares the power control voltage PWR CNTL divided by resistors R0717 to R0719 with the voltage limit setting VLTG LIMIT SET from the D/A converter (U0731-13) and keeps the control voltage constant via Q0711 if the control voltage, reduced by the resistive divider (R0717 to R0719), approaches the voltage of VLTG LIMIT SET (U0731-13).

Rise and fall time of the output power during transmitter keying and dekeying is controlled by the comparator formed by opamp U0701-3.

During normal transmitter operation the voltage at U701-3 pin 13 is higher than the voltage at pin 12 causing the output at pin 14 being low and switching off transistor Q0711. Diode D0732 reduces the bias voltage BIAS VLTG for low control voltage levels.

The temperature of the PA area is monitored by opamp U0701-1 using thermistor R5641 (located in the PA section). If the temperature increases, the resistance of R5641 decreases, decreasing the voltage PA TEMP. The inverting amplifier formed by U0701-1 amplifies the PA TEMP voltage and if the voltage at opamp pin 1 approaches 4.6 V plus the voltage (ON) across D0721, U701-1 simulates an increased power which in turn decreases the power control voltage until the voltage at U0701-4 pin 9 is 4.6V again. During normal transmitter operation the output voltage of opamp U701-1 pin 1 is below 4.6V. Diode D5601 located in the PA section acts as protection against transients and wrong polarity of the supply voltage.

10.0 Frequency Synthesis

The complete synthesizer subsystem consists of the Reference Oscillator (U7502), the Fractional-N synthesizer (U7501), the Voltage Controlled Oscillator (Q5741, Q5751), the RX and TX buffer stages (Q5771, Q5781) and the feedback amplifier (Q5791).

10.1 Reference Oscillator

The Reference Oscillator (Y5702) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. An analog to digital (A/D) converter internal to U5701 (FRAC-N) and controlled by the microprocessor via serial interface (SRL) sets the voltage at the warp output of U5701 pin 16 to set the frequency of the oscillator. The output of the oscillator (pin 2 of Y5702) is applied to pin 14 (XTAL1) of U5701 via a RC series combination.

In applications were less frequency stability is required the oscillator inside U5701 is used along with an external crystal Y5701, the varactor diode D5702, C5708, C5710 and R5704.

10.2 Fractional-N Synthesizer (U7501)

The FRAC-N synthesizer IC (U7501) consists of a pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balance attenuator to balance the high frequency analog modulation and low frequency digital modulation, a 13V positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 9.3 volts.

A voltage of 9.3V applied to the super filter input (U7501 pin 22) supplies an output voltage of 8.6 VDC at pin 18. It supplies the VCO (Q5741), VCO modulation bias circuit (via R5714) and the synthesizer charge pump resistor network (R5723, R5724, R5726). The synthesizer supply voltage is provided by the 5V regulator U5801.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U5701-32), a voltage of 13 VDC is being generated by the positive voltage multiplier circuitry (D5701-1-3, C5716, C5717). This voltage multiplier is basically a diode capacitor network driven by two (1.05MHz) 180 degrees out of phase signals (U5701-9 and -10).

Output LOCK (U5701-2) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. IC U5701 divides the 16.8 MHz reference frequency down to 2.1 MHz and provides it at pin 11. This signal is used as clock signal by the controller.

The serial interface (SRL) is connected to the microprocessor via the data line SPI DATA (U5701-5), clock line SPI CLK (U5701-6), and chip enable line FRACN CE (U5701-7).

10.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) is formed by the colpitts oscillator FET Q5741. Q5741 draws a drain current of 12 mA from the FRAC-N IC super filter output. The oscillator frequency is half of the desired frequency and mainly determined by L5743, C5742, C5743, C5745 - C5748 and varactor diodes D5741 / D5742. Diode D5743 controls the amplitude of the oscillator.

A balanced frequency doubler T5751, D5751 converts the oscillator fundamental to the desired UHF frequency. With a steering voltage from 2.5V to 10.5V at the varactor diodes the full RX and TX frequency range from 357.9 MHz to 470 MHz is covered.

After the doubler a 3-pole bandpass filter rejects unwanted harmonics at the first and third oscillator fundamental frequency and matches the output to the Common VCO Buffer Q5751. Q5751 draws a collector current of 13 mA from the stabilized 5V (U5801) and drives the Pre-scaler Buffer Q5791, the PA Buffer Q5781 (Pout = 13dBm) and Mixer Buffer Q5771 (Pout = 10dBm). Q5791 draws a collector current of 8 mA from the stabilized 5V and Q5771, Q5781 both draw 17mA form the 9V3 source. The buffer stages Q5771, Q5781 and the feedback amplifier Q5791 provide the necessary gain and isolation for the synthesizer loop.

Q5731 is controlled by output AUX3 of U7501 (pin 1) and enables the RX or TX buffer. In RX mode AUX3 is nearly at ground level, in TX mode about 5V DC. In TX mode with R5732 pulled to ground level by Q5731 the modulation signal coming from the FRAC-N synthesizer IC (U7501 pin28) modulates the VCO via varactor diode D5731 while in RX mode the modulation circuit is disabled by pulling R5732 to a higher level through R5772.

10.4 Synthesizer Operation

The complete synthesizer subsystem works as follows. The output signal of the VCO (Q5741) is frequency doubled by doubler D5751 and, buffered by Common VCO Buffer Q5751. To close the synthesizer loop, the collector of Q5791 is connected to the PREIN port of synthesizer U5701 (pin 20). The buffer output (Q5751) also provides signals for the Mixer Buffer Q5771 and the PA Buffer (Q5781).

The pre-scaler in the synthesizer (U5701) is basically a dual modulus pre-scaler with selectable divider ratios. This divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SRL. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider´s output signal with the reference signal.The reference signal is generated by dividing down the signal of the reference oscillator (Y5702).

The output signal of the phase detector is a pulsed DC signal which is routed to the charge pump. The charge pump outputs a current at pin 29 (I OUT of U5701). The loop filter (which consists of R5715-R5717, C5723-C5725, C5727) transforms this current into a voltage that is applied to the varactor diodes D5741, D5742 and alters the output frequency of the VCO. The current can be set to a value fixed in the FRAC-N IC or to a value determined by the currents flowing into CPBIAS 1 (U5701-27) or CPBIAS 2 (U5701-26). The currents are set by the value of R5724 or R5726 respectively. The selection of the three different bias sources is done by software programming.

To reduce synthesizer lock time when new frequency data has been loaded into the synthesizer the magnitude of the loop current is increased by enabling the IADAPT line (U5701-31) for a certain software programmable time (Adapt Mode). The adapt mode timer is started by a low to high transient of the FRACN CE line. When the synthesizer is within the lock range the current is determined only by the resistors connected to CPBIAS 1, CPBIAS 2, or the internal current source.

A settled synthesizer loop is indicated by a high level of signal LOCK DET (U5701-2). This signal is routed to uP U0101-17 for further processing.

In order to modulate the PLL the two spot modulation method is utilized. Via pin 8 (MODIN) on U5701 the audio signal is applied to both the A/D converter (low freq path) as well as the balance attenuator (high freq path). The A/D converter converts the low frequency analog modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U5701-28) and connected to the VCO modulation diode D5731.

VHF SPECIFIC CIRCUIT DESCRIPTION

11.0 Receiver Front-End

The receiver is able to cover the VHF range from 136 to 174 MHz. It consists of four major blocks: front-end, mixer, first IF section and IF IC. Antenna signal pre-selection is performed by two varactor tuned bandpass filters. A double balanced schottky diode mixer converts the signal to the first IF at 45.1 MHz.

Two crystal filters in the first IF section and two ceramic filters in the second IF section provide the required selectivity. The second IF at 455 kHz is mixed, amplified and demodulated in the IF IC. The processing of the demodulated audio signal is performed by an audio processing IC located in the controller section.

11.1 Front-End Band-Pass Filter and Pre-Amplifier

A two pole pre-selector filter tuned by the dual varactor diode D3301 pre-selects the incoming signal (PA RX) from the antenna switch to reduce spurious effects to following stages. The tuning voltage (FE CNTL VLTG) ranging from 2 volts to 8 volts is controlled by a Digital to Analog (D/A) converter (U0731-11) in the controller section. A dual hot carrier diode (D3303) limits any inband signal to 0dBm to prevent damage to the pre-amplifier.

The RF pre-amplifier is an SMD device (Q3301) with collector base feedback to stabilize gain, impedance, and intermodulation. The collector current of approximately 11-16 mA, drawn from the voltage 9V3, is controlled by a current source composed of Q3302, R3302, R3300, and R3311 - R3313. In transmit mode the high K9V1 signal fed through diode D3300 switches off the current source and in turn the pre-amplifier. In receive mode K9V1 must be low to switch on the current source. A 3 dB pad (R3306 - R3308 and R3316 - R3318) stabilizes the output impedance and intermodulation performance.

A second two pole varactor tuned bandpass filter provides additional filtering to the amplified signal. The dual varactor diode D3304 is controlled by the same signal which controls the pre-selector filter.

If the VHF radio is configured for a base station application, R3318 is not placed and TP3301 and TP3302 are shorted.

11.2 Mixer and Intermediate Frequency (IF) Section

The signal coming from the front-end is converted to the first IF (45.1 MHz) using a double balanced schottky diode mixer (D3331). Its ports are matched for incoming VHF signal conversion to the 45.1MHz IF using high side injection. The injection signal (VCO MIXER) coming from the mixer buffer (Q3770) is filtered by the lowpass consisting of (L3333, L3334, C3331 - C3333) and has a level of approximately 10 dBm.

The mixer IF output signal (RX IF) from transformer T3301 pin 2 is fed to the first two pole crystal filter Y5201. The filter output in turn is matched to the following IF amplifier.

The IF amplifier Q5201 is actively biased by a collector base feedback (R5201, R5202) to a current drain of approximately 5 mA drawn from the voltage 5V STAB. The output impedance is matched to the second two pole crystal filter Y5202. A dual hot carrier diode (D5201) limits the filter output voltage swing to reduce overdrive effects at RF input levels above -27 dBm.

11.3 IF IC (U5201)

The first IF signal from the crystal filters feeds the IF IC (U5201) at pin 6. Within the IF IC the 45.1MHz first IF signal mixes with the second local oscillator (LO) at 44.645MHz to the second IF at 455 kHz. The second LO uses the external crystal Y5211. The second IF signal is amplified and filtered by two external ceramic filters (FL5201, FL5202). Back in the IF IC the signal is demodulated in a phase-lock detector and fed from IF IC pin 28 to the audio processing circuit AFIC U0103 located in the controller section (line DET AUDIO).

The IF IC also controls the squelch characteristics of the radio. With a few external parts (R5222, C5229, C5230, R5223) the squelch tail, hysteresis, attack and delay were optimized for the radio. To set the squelch threshold the signal from IF IC pin 23 (line SQ ATT IN) is attenuated by a microprocessor controlled audio processing IC AFIC (U0103) located in the controller section. The attenuated signal from the AFIC (line SQ ATT OUT) enters the IF IC at pin 20 and is used to create a squelch indicator signal available at pin 15 (CSQ DET).

The microprocessor controlled ADAPT signal at pin 22 activates the fast squelch indicator signal at IF IC pin 18 (FAST SQ). Both squelch indicator signals CSQ DET (pin 15) and FAST SQ (pin 18) are combined, weighted by R0111 / R0112 and fed to the microprocessor U0101 pin 15 for interpretation. From the voltage weighted by the resistors the µP determines whether CSQ DET, FAST SQ or both are active.

At IF IC pin 11 an RSSI signal is available with a dynamic range of 70 dB. The RSSI signal is buffered by op-amp U0106-3 and available at accessory connector J0400-15.

12.0 Power Amplifier (PA) 5-25W

The radio's 5-25 W PA is a three stage amplifier used to amplify the output from the exciter to the radio transmit level. It consists of three stages in the line-up. The first (Q3511) is a bipolar stage that is controlled via the PA control line. It is followed a MOS FET stage (Q3521) and a final bipolar stage (Q3531).

Devices Q3511 and Q3521 are surface mounted. Bipolar Transistor Q3531 is directly attached to the heat sink.

12.1 Power Controlled Stage

The first stage (Q3511) amplifies the RF signal from the VCO (line EXCITER PA) and controls the output power of the PA. The output power of the transistor Q3511 is proportional to its collector current which is adjusted by a voltage controlled current source consisting of Q3641 and Q3642. The current of the whole stage is drawn from the RX-TX Switch through coil L3652.

The collector current of Q3511 causes a voltage drop across the resistors R3645 and R3646. Transistor Q3641 adjusts the voltage drop across R3644 through PA control line (PWR CNTL). The current source Q3642 adjusts the collector current of Q3511 by modifying its base voltage until the voltage drop across R3645 and R3646 plus VBE (0.6V) equals the voltage drop across R3644. If the voltage of PWR CNTL is raised, the base voltage of Q3641 will also rise causing more current to flow to the collector of Q3641 and a higher voltage drop across R3644. This in turn results in more current driven into the base of Q3511 by Q3642 so that the current of Q3511 is increased. The collector current settles when the voltage over the series configuration of R3645 and R3646 plus VBE of Q3642 equals the voltage over R3644. By controlling the output power of Q3511 and in turn the input power of the following stages the ALC loop is able to regulate the output power of the transmitter.

In receive mode the PA control line (PWR CNTL) is at ground level and switches off the collector current of Q3641 which in turn switches off the current source transistor Q3642 and the RF transistor Q3511.

12.2 PA Stages

The following stage uses an enhancement mode N-Channel MOS FET device (Q3521) and requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line BIAS VLTG is set in transmit mode by a Digital to Analog (D/A) converter (U0731-4) and fed to the gate of Q53521 via the resistive network R3613 - R3615. The bias voltage is tuned in the factory. If the transistor is replaced, the bias voltage must be tuned with the Radio Service Software (RSS). Care must be taken, not to damage the device by exceeding the maximum allowed bias voltage. The collector current is drawn from the supply voltage 9V3 SUPP.

The final stage uses the bipolar device Q3531 and operates off the A+ supply voltage. For class C operation the base is DC grounded by two series inductors (L3521, L3522). A matching network consisting of C3530-C3534, L3532, L3533 and two striplines transform the impedance to 50 Ohms and feed the directional coupler.

12.3 Directional Coupler

The directional coupler is a microstrip printed circuit which couples a small amount of the forward power off the RF power from Q3531. The coupled signal is rectified to an output power proportional negative DC voltage by the diode D3657 and sent to the power control circuit in the controller section via the line PWR DETECT for output power control. The power control circuit holds this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

12.4 Antenna Switch

The antenna switch is switched synchronously with the PWR CNTL signal and feeds either the antenna signal coming through the harmonic filter to the receiver or the transmitter signal coming from the PA to the antenna via the harmonic filter.

In transmit mode, this PWR CNTL signal is above 1 V and biases Q3511 through Q3641 and Q3642 to allow a collector current to be drawn. The collector current of Q3511 drawn from A+ flows via L3631, L3531, L3532, L3533, directional coupler, D3551, L3651, D3651, L3652, Resistors R3645, R3646, R3648 and switches the PIN diodes D3551 and D3651 to the low impedance state. D3551 leads the RF signal from the directional coupler to the harmonic filter. The low impedance of D3651 is transformed to a high impedance at the input of the harmonic filter by the resonant circuit formed by L3651,C3652 and the input capacitance of the harmonic filter.

In receive mode the PWR CNTL signal at ground level turns off the current through the PIN diodes and switches them to the high impedance state. The antenna signal, coming through the harmonic filter, is channelled to the receiver via L3651, C3651 and line PA RX. The high impedance of D3651 in off state does not influence the receiver signal.

12.5 Harmonic Filter

The transmitter signal from the antenna switch is channelled through the harmonic filter to the antenna connector J3501.The harmonic filter is formed by inductors L3551, L3552, and capacitors C3551 - C3554 This network forms a low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R3551 is used for electro - static protection.

12.6 Power Control

The power control loop regulates transmitter power with an automatic level control (ALC) loop and provides protection features against excessive control voltage and high operating temperatures.

MOS FET device bias, power and control voltage limit are adjusted under microprocessor control using a Digital to Analog (D/A) converter (U0731). The microprocessor writes the data into the D/A converter via serial interface (SRL) composed of the lines SPI CLCK SRC (clock), SPI DATA SRC (data) and DAC CE (chip enable). The D/A adjustable control voltage limit increases transmitter rise time and reduces adjacent channel splatter as it is adjusted closer to the actual operating control voltage.

The microprocessor controls K9V1 ENABLE (U0101-6) to switch on the first and the second PA stage via K9V1. The antenna switch is turned on by the collector current of the first PA stage. PA DISABLE, also microprocessor controlled (U0101-54), sets BIAS VLTG (U0731-4) and VLTG LIMIT SET (U0731-13) in receive mode to low to switch off the bias of the MOS FET device Q3521 and to switch off the power control voltage (PWR CNTL).

Through an Analog to Digital (A/D) input (VLTG LIMIT) the microprocessor can read the PA control voltage (PWR CNTL) during the tuning process.

The ALC loop regulates power by adjusting the PA control line PWR CNTL to keep the forward power voltage PWR DETECT at a constant level.

Opamp U0701-2 and resistors R0701 to R0703 and R0731 subtract the negative PWR DETECT voltage from the PWR SET D/A output U0731 pin 2. The result is connected to opamp inverting input U0701-4 pin 9. This voltage which is compared with a 4.6 volt reference VAG present at noninverting input U0701-4 pin 10 and controls the output power of the PA via pin 8 and control line PWR CNTL. The 4.6 volt reference VAG is set by a resistive divider circuit (R0171, R0172) which is connected to ground and 9.3 volts and buffered by opamp U0105-1.

During normal transmitter operation the voltages at the opamp inputs U0701-4 pins 9 and 10 should be equal to 4.6 volts and the PA control voltage output at pin 8 should be between 4 and 7 volts. If power falls below the desired setting, PWR DETECT increases, causing the output at U0701-2 pin 7 to decrease and the opamp output U0701-4 pin 8 to increase.

A comparator formed by U0701-4 increases the PA control voltage PA CNTL until PWR DETECT is at the desired level. The power set D/A output voltage PWR SET (U0731-2) at U0701-2 pin 5 adjusts power in steps by adjusting the required value of PWR DETECT. As PWR SET (U0731-2) decreases, transmitter power must increase to make PWR DETECT larger and keep the inverting input U0701-4 pin 9 at 4.6 volts.

Loop frequency response is controlled by opamp feedback components R0712 and C0711. Opamp U0701-3 compares the power control voltage PWR CNTL divided by resistors R0717 to R0719 with the voltage limit setting VLTG LIMIT SET from the D/A converter (U0731-13) and keeps the control voltage constant via Q0711 if the control voltage, reduced by the resistive divider (R0717 to R0719), approaches the voltage of VLTG LIMIT SET (U0731-13).

Rise and fall time of the output power during transmitter keying and dekeying is controlled by the comparator formed by opamp U0701-3.

During normal transmitter operation the voltage at U701-3 pin 13 is higher than the voltage at pin 12 causing the output at pin 14 being low and switching off transistor Q0711. Diode D0732 reduces the bias voltage BIAS VLTG for low control voltage levels.

The temperature of the PA area is monitored by opamp U0701-1 using thermistor R3611 (located in the PA section). If the temperature increases, the resistance of R3611 decreases, decreasing the voltage PA TEMP. The inverting amplifier formed by U0701-1 amplifies the PA TEMP voltage and if the voltage at opamp pin 1 approaches 4.6 V plus the voltage (ON) across D0721, U701-1 simulates an increased power which in turn decreases the power control voltage until the voltage at U0701-4 pin 9 is 4.6V again. During normal transmitter operation the output voltage of opamp U701-1 pin 1 is below 4.6V. Diode D3601 located in the PA section acts as protection against transients and wrong polarity of the supply voltage.

13.0 Frequency Synthesis

The complete synthesizer subsystem consists of the Reference Oscillator (Y3702 or Y3701), the Fractional-N synthesizer (U3701), the Voltage Controlled Oscillator (Q3741, Q3751), the RX and TX buffer stages (Q3760, Q3770, Q3780) and the feedback amplifier (Q3790).

13.1 Reference Oscillator

The Reference Oscillator (Y3702) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. An analog to digital (A/D) converter internal to U3701 and controlled by the microprocessor via serial interface (SRL) sets the voltage at the warp output of U3701 pin 16 to set the frequency of the oscillator. The output of the oscillator (pin 2 of Y3702) is applied to pin 14 (XTAL1) of U3701 via a RC series combination.

In applications were less frequency stability is required the oscillator inside U3701 is used along with an external crystal Y3701, the varactor diode D3702, C3708, C3710 and R3704.

13.2 Fractional-N Synthesizer (U3701)

The FRAC-N synthesizer IC (U3701) consists of a pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balance attenuator to balance the high frequency analog modulation and low frequency digital modulation, a 13V positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 9.3 volts.

A voltage of 9.3V applied to the super filter input (U3701 pin 22) supplies an output voltage of 8.6 VDC at pin 18. It supplies the VCO (Q3741 / Q3751), VCO modulation bias circuit (R3714) and the synthesizer charge pump resistor network (R3723, R3724). The synthesizer supply voltage is provided by the 5V regulator U3801.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U3701-32), a voltage of 13 VDC is being generated by the positive voltage multiplier circuitry (D3701-1-3, C3716, C3717). This voltage multiplier is basically a diode capacitor network driven by two (1.05 MHz) 180 degrees out of phase signals (U3701-9 and -10).

Output LOCK (U3701-2) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. IC U3701 divides the 16.8 MHz reference frequency down to 2.1 MHz and provides it at pin 11. This signal is used as clock signal by the controller.

The serial interface (SRL) is connected to the microprocessor via the data line SPI DATA (U3701-5), clock line SPI CLK (U3701-6), and chip enable line FRACN CE (U3701-7).

13.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) uses 2 colpitts oscillators, FET Q3741 for transmit and FET Q3751 for receive. The appropriate oscillator is switched on or off by FRAC-N IC output AUX3 (U3701-1) using transistors Q3742 and Q3752. In RX mode AUX3 is nearly at ground level and Q3742 enables a current flow from the source of FET Q3751 while Q3752 is switched off. In TX mode AUX3 is about 5V DC and Q3742 is switched off. Q3752 is switched on and enables a current flow from the source of FET Q3741 while Q3751 is switched off. When switched on the FETs draw a drain current of 8 mA from the FRAC-N IC super filter output. The frequency of the receive oscillator is mainly determined by L3752, C3752, C3754 - C3756 and varactor diodes D3751 / D3752. Diode D3754 controls the amplitude of the oscillator. The frequency of the transmit oscillator is mainly determined by L3734, C3736 - C3740 and varactor diodes D3732 / D3733. Diode D3739 controls the amplitude of the oscillator. With a steering voltage from 3V to 10V at the varactor diodes the RX frequency range from 181.1 MHz to 219.1 MHz and the TX frequency range from 136 MHz to 174 MHz are covered. In TX mode the modulation signal coming from the FRAC-N synthesizer IC (U3701 pin 28) modulates the TX VCO via varactor diode D3731.

Both oscillator outputs are combined and buffered by the VCO Buffer Q3760. Q3760 draws a collector current of 13 mA from the stabilized 5V (U3801) and drives the Mixer Buffer Q3770. Q3770 draws a collector current of 17 mA from the 9V3 voltage and drives the PA Buffer Q3780 (Pout = 13dBm) and the Pre-scaler Buffer Q3790. Q3790 draws a collector current of 8 mA from the stabilized 5V (U3801) and drives the pre-scaler internal to the FRAC-N IC. In transmit mode Q3780 is switched on by the K9V1 signal and draws a collector current of 19 mA from the K9V1 voltage. The injection signal VCO MIXER with a level of 10dBm feeds the mixer through R3774. The buffer stages Q3760, Q3770, Q3780 and the feedback amplifier Q3790 provide the necessary gain and isolation for the synthesizer loop.

13.4 Synthesizer Operation

The complete synthesizer subsystem works as follows. The combined output signal of the RX VCO (Q3751) and TX VCO (Q3741) is buffered by VCO Buffer Q3760, Mixer Buffer Q3770 and Pre-scaler Buffer Q3790. To close the synthesizer loop, the collector of Q3790 is connected to the PREIN port of synthesizer U3701 (pin 20). The output of (Q3770) also provides signals for the mixer (via VCO MIXER) and the PA Buffer (Q3780).

The pre-scaler in the synthesizer (U3701) is basically a dual modulus pre-scaler with selectable divider ratios. This divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SRL. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider´s output signal with the reference signal.The reference signal is generated by dividing down the signal of the reference oscillator (Y3702).

The output signal of the phase detector is a pulsed DC signal which is routed to the charge pump. The charge pump outputs a current at pin 29 (I OUT of U3701). The loop filter (which consists of R3715 - R3717, C3723 - C3725, C3727) transforms this current into a voltage that is applied to the varactor diodes D3732, D3733 (TX), D3751, D3752 (RX) and alters the output frequency of the TX VCO (Q3741) and RX VCO (Q3751). The current can be set to a value fixed in the FRAC-N IC or to a value determined by the current flowing into CPBIAS 1 (U3701-27). The current is set by the value of R3723 and R3724. The selection of the two different bias sources is done by software programming.

To reduce synthesizer lock time when new frequency data has been loaded into the synthesizer the magnitude of the loop current is increased by enabling the IADAPT line (U3701-31) for a certain software programmable time (Adapt Mode). The adapt mode timer is started by a low to high transient of the FRACN CE line. When the synthesizer is within the lock range the current is determined only by the resistors connected to CPBIAS 1 or the internal current source.

A settled synthesizer loop is indicated by a high level of signal LOCK DET (U3701-2). This signal is routed to µP U0101-17 for further processing.

In order to modulate the PLL the two spot modulation method is utilized. Via pin 8 (MODIN) on U3701 the audio signal is applied to both the A/D converter (low freq path) as well as the balance attenuator (high freq path). The A/D converter converts the low frequency analog modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U3701-28) and connected to the VCO modulation diode D3731.

Chapter 5

Control Heads/UHF/VHF Diagrams and Parts Lists

Table of Contents

Description Page

Control Head Diagrams and Parts Lists

Control Head - Model A2, PCB Layouts 1
Control Head - Model A2, Schematic Diagram 3
Parts List 4
Control Head - Model A3, PCB Layouts 5
Control Head - Model A3, Schematic Diagram 7
Parts List 8

UHF (403-470MHz) Diagrams and Parts Lists

PCB Layout Component Side 9
PCB Layout Solder Side 10
128ch Model, Controller Schematic Diagram *1 of 2* 11
128ch Model, Controller Schematic Diagram *2 of 2* 13
Parts List 12/14
4ch Model, Controller Schematic Diagram *1 of 2* 15
4ch Model, Controller Schematic Diagram *2 of 2* 17
Parts List 16/18
Supply Voltage Schematic Diagram. 19
Parts List 20
Power Control Schematic Diagram 21
Parts List 22
Power Amplifier 5-25W Schematic Diagram 23
Parts List 24
Synthesizer Schematic Diagram 25
Parts List 26
Voltage Controlled Oscillator Schematic Diagram 27
Parts List 28

Description Page

RX-FE Schematic Diagram 29
Parts List. 30
RX-IF Schematic Diagram. 31
Parts List. 32

VHF (136-174MHz) Diagrams and Parts Lists

PCB Layout Component Side. 33
PCB Layout Solder Side. 34
128ch Model, Controller Schematic Diagram *1 of 2* 35
128ch Model, Controller Schematic Diagram *2 of 2* 37
Parts List. 36/38
4ch Model, Controller Schematic Diagram *1 of 2* 39
4ch Model, Controller Schematic Diagram *2 of 2* 41
Parts List. 40/42
Supply Voltage Schematic Diagram 43
Parts List. 44
Power Control Schematic Diagram. 45
Parts List. 46
Power Amplifier 5-25W Schematic Diagram. 47
Parts List. 48
Synthesizer Schematic Diagram 49
Parts List. 50
Voltage Controlled Oscillator Schematic Diagram 51
Parts List. 52
RX-FE Schematic Diagram 53
Parts List. 54
RX-IF Schematic Diagram. 55
Parts List. 56

MOTOROLA

GM350

Mobile Radio

Service Manual

300-345MHz Specific Information

CHAPTER 6



Chapter 6

300-345MHz Specific Information

Table of Contents

Chapter

6.1 Model Chart and Test Specifications 6.1-1

6.2 Radio Tuning Procedure 6.2-1

6.3 Theory of Operation 6.3-1

6.4 Diagrams and Parts Lists.....6.4-1

Chapter 6.1

Model Chart and Test Specifications

Table of Contents

Paragraph		Page
1.0	**Overview**	1
2.0	**Model Chart**	1
3.0	**GM350 Technical Specification**	2
3.1	General	2
3.2	Transmitter	2
3.3	Receiver	3

1.0 Overview

This chapter lists the models and the technical specifications for the GM350 mobile radio.

2.0 Model Chart

	Description	GM350 300-345MHz 12.5 kHz 25W	GM350 300-345 MHz 12.5 kHz 25W D	GM350 300-345 MHz 20/25 kHz 25W	GM350 300-345 MHz 20/25 kHz 25W D	**GM350 300-345 MHz (Tx:300-345 Rx: 300-350)** X = Indicates one of each required	
	Model	M08EHE4AA2AN	M08EHF4AA3AN	M08EHE6AA2AN	M08EHF6AA3AN		
						Item	**Description**
		X	X	X	X	GBN6147	Packaging Kit
		X		X		GCN6103	Control Head Model A2 Non-Display
			X		X	GCN6105	Control Head Model A3 Display
		X	X	X	X	GLN7324	Low Profile Trunnion Kit
		X	X	X	X	GMN6146	Enhanced Compact Microphone
		X				GUD1312	RF & HSG 4ch 12.5kHz 5-25W
				X		GUD1313	RF & HSG 4ch 20/25kHz 5-25W
			X			GUD1310	RF & HSG 128ch 12.5kHz 5-25W
					X	GUD1311	RF & HSG 128ch 20/25kHz 5-25W
		X	X	X	X	GKN6270	Power Cable
		X	X	X	X	68P02923X01	GM350 User Guide M/L

3.0 GM350 Technical Specification

3.1 General

SPECIFICATION ITEM	TYPICAL VALUE
Frequency Range	Tx: 300-345MHz Rx: 300-350MHz
Channel Spacing	12.5 or 20/25 kHz
Frequency Stability	±2ppm
Power Supply	10.8 to 15.6V dc, negative earth
Dimensions	44x168x160 mm (HxWxD)
Weight	1030g
Operational Temperature	- 25°C to + 55°C
Storage Temperature	- 40°C to + 85°C
Antenna Connection	50Ω BNC
Environmental - Mechanical - Electrical	 Vibration IEC 68/2/27 and Shock IEC 28/2/6 European Dust & Water protection IP54 ETS300-086 RF Specifications ETS300-113 Cyclic Keying Requirements ETS300-279 EMC Requirements ETS300-219 Signalling

3.2 Transmitter

SPECIFICATION ITEM	TYPICAL VALUE
Channel Spacing	12.5 or 20/25 kHz
Output Power	5-25W
Modulation Limiting	<±2.5kHz (12.5kHz); <±4kHz (20kHz); <±5kHz (25kHz)
FM hum & noise (CCITT)	>40dB (12.5kHz); >45dB (25kHz) CCITT
Conducted/Radiated Emission	<0.25uW (0.1...1000MHz); <1uW (1...4GHz)
Adjacent Channel Power	<-60dB (12.5kHz); <-70dB (25kHz)
Audio Response (300 - 3000 Hz)	Flat or pre-emphasised
Audio Distortion	<5% @ 1kHz, 60% deviation
Transmit turn on time	<25msec

3.3 Receiver

SPECIFICATION ITEM	TYPICAL VALUE
Channel Spacing	12.5 or 20/25 kHz
Sensitivity @ 12.5 kHz	< 0.35uV (12dB SINAD)
Sensitivity @ 25 kHz	< 0.35uV (12dB SINAD)
Intermodulation	>65dB ETS; >70dB with Base Option
Adjacent Channel Selectivity	>60dB (12.5kHz); >70dB (20/25kHz) ETS
Spurious Rejection	>70dB ETS
Audio Distortion @ Rated Audio	<5%
Hum and Noise (CCITT)	>40dB (12.5kHz); >45dB (20/25kHz) CCITT
Audio Response (300 - 3000 Hz)	Flat or De-Emphasised
Co-channel Rejection	<12dB (12.5kHz) , <8dB (20/25kHz) ETS
Conducted /Radiated Emission	<2nW (0,1..1000MHz); <20nW (1..4GHz)
Receive after transmit time	<25msec
Audio Output Power	4W (internal speaker); <13W external

Chapter 6.2

Radio Tuning Procedure

Table of Contents

Paragraph		Page
1.0	**Radio Tuning Procedure**	1
1.1	General	1
1.2	PA Bias Voltage	2
1.3	Battery Threshold	3
1.4	Transmitter Power	3
1.5	Reference Oscillator	4
1.6	Front-End Pre-Selector	4
1.7	Rated Volume	5
1.8	Squelch	5
1.9	Transmit Deviation Limit	6
1.10	Transmit Modulation Balance (Compensation)	7

1.0 GM350 Radio Tuning

1.1 General

The recommended hardware platform is a 386 or 486 DX 33 PC (personal computer) with 8 MBytes RAM, MS DOS 5.0, Windows 3.1, and RSS (Radio Service Software). These are required to align the radio. Refer to your RSS Installation Manual for installation and setup procedures for the required software; the user manual is accessed (and can be printed if required) via the RSS.

To perform the alignment procedures, the radio must be connected to the PC, RIB (Radio Interface Box), and Universal Test Set as shown in figure 6.2-1.

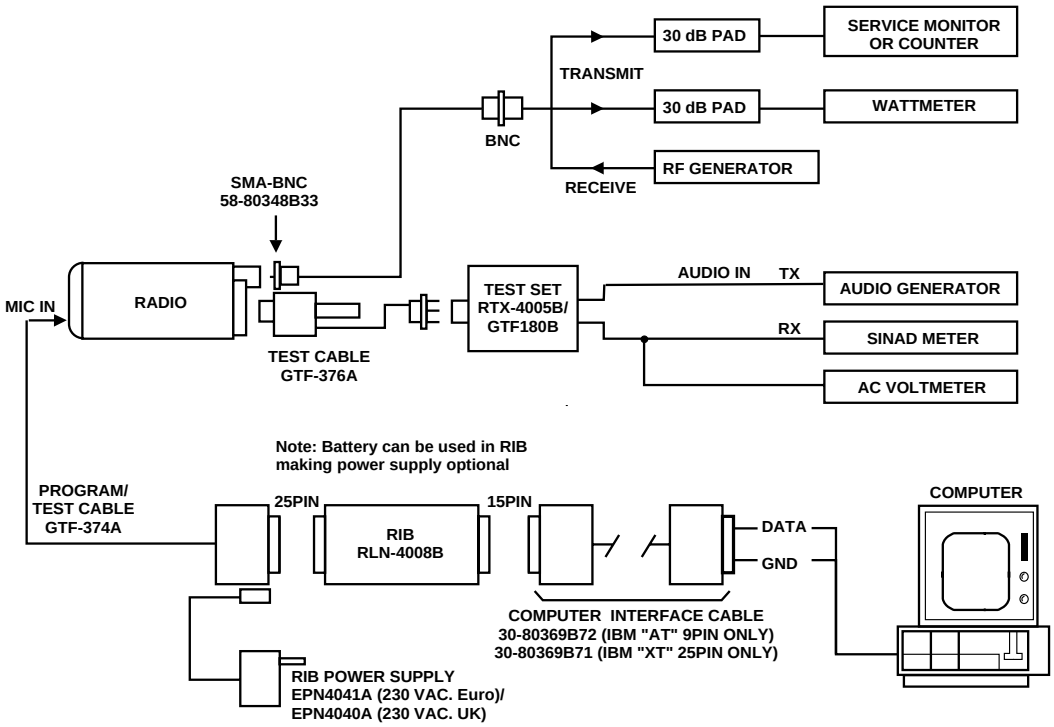


Figure 6.2-1 Radio Alignment Test Setup.

All tuning procedures are performed from the Service menu.

Before going into the Service menu, the radio must first be read using the File / Read Radio menu (if the radio has just been programmed with data loaded from disk or from a newly created codeplug, then it must still be read so that the RSS will have the radio's actual tuning values).

All Service windows read and program the radio codeplug directly; you do NOT have to use the RSS Read Radio / Write Radio functions to program new tuning values.

CAUTION:



DO NOT switch radios in the middle of any Service procedure. Always use the Program or Cancel key to close the tuning window before disconnecting the radio. Improper exits from the Service window may leave the radio in an improperly configured state and result in seriously degraded radio or system performance.

The Service windows introduce the concept of the “Softpot”, an analog SOFTware controlled POTentiometer used for adjusting all transceiver alignment controls. A softpot can be selected by clicking with the mouse at the value or the slider or by hitting the TAB key until the value or the slider is highlighted.

Each Service window provides the capability to increase or decrease the ‘softpot’ value with the mouse, the arrow keys or by entering a value with the keyboard. The window displays the minimum, maximum, and step value of the softpot. In addition transmitter tuning windows indicate the transmitter frequency and whether the radio is keyed.

Adjusting the softpot value sends information to the radio to increase (or decrease) a DC voltage in the corresponding circuit. For example, increasing the value in the Reference Oscillator tune window instructs the radio microprocessor to increases the voltage across a varactor in the reference oscillator to increase the frequency. Pressing the Program button stores all the softpot values of the current window permanently in the radio.

In ALL cases, the softpot value is just a relative number corresponding to a D/A (Digital-to-Analog) generated voltage in the radio. All standard measurement procedures and test equipment are similar to previous radios.

Refer to the RSS on-line help for information on the tuning software.
Perform the following procedures in the sequence indicated.

Note: All tuning procedures must be performed at a supply voltage of 13.2V unless otherwise stated. The Modulation Analyser to measure the deviation should be set to frequency modulation with de-emphasis switched off and all high pass filters switched off.

1.2 PA Bias Voltage

Adjustment of the PA Bias is critical for proper radio operation. Improper adjustment will result in poor operation and may damage the PA FET device. For this reason, the PA bias must be set before the transmitter is keyed the first time.

1. From the Service menu, select Tx Alignment.
2. Select Bias Voltage to open the bias voltage tuning window. If the control voltage is out of range, an error message will be displayed. In this case the radio hardware has a problem and tuning must be stopped immediately.
3. Press the Toggle Bias button to set the quiescent current temporarily to 0 mA. The status bar will indicate that the bias is switched off.
4. Measure the DC current of the radio. Note the measured value and add the specified quiescent current shown in table 6.2-1. The result is the tuning target.
5. Press the Toggle Bias button to switch on the quiescent current again.
6. Adjust the current per the target calculated in step 4.
7. Press Program to store the softpot value.
8. For 300-345MHz: Repeat procedure for Bias Voltage 2.

Table 6.2-1 Quiescent Current Alignment.

RF-Band	Target
300-345MHz	150mA±15%

1.3 Battery Threshold

The radio uses 2 battery threshold levels Tx High and Tx Low to determine the battery condition.

1. From the Service menu, select Tx Alignment.
2. Select Battery Thresholds to open the battery thresholds tuning window.
3. Set the supply voltage to the value indicated for Tx High.
4. Press the Tx High Program button to store the softpot value for Tx High.
5. Set the supply voltage to the value indicated for Tx Low.
6. Press the Tx Low Program button to store the softpot value for Tx Low.
7. Close the window by pressing Cancel.

1.4 Transmitter Power

IMPORTANT: To set the transmitter power for customer applications use the Per Radio window under the Edit menu and set the “Level 1” and “Level 2” powers to the desired values. Only if the transmitter components have been changed should the following procedure be performed.

The advanced power setting technology employed in the GM350 makes use of two reference power level settings along with parameters describing the circuit behaviour. To set the reference points requires tuning on two power level settings, a high power level setting, and a low power level setting.

1. From the Service menu, select Tx Alignment.
2. Select RF Power to open the RF power tuning window. The window will indicate the transmit test frequencies to be used.
3. Select Point 1 value of the first frequency.
4. Press Toggle PTT to key the radio. The status bar will indicate that the radio is transmitting.
5. Measure the transmitter power on your power meter.
6. Enter the measured value in the box Point 1.
7. Select Point 2 value of the first frequency.
8. Measure the transmitter power on your power meter.
9. Enter the measured value in the box Point 2.
10. Press Toggle PTT to dekey the radio.
11. Repeat steps 3 - 10 for all test frequencies shown in the window.
12. Press Program to store the softpot values.

1.5 Reference Oscillator

Adjustment of the reference oscillator is critical for proper radio operation. Improper adjustment will not only result in poor operation, but also a misaligned radio that will interfere with other users operating on adjacent channels. For this reason, the reference oscillator should be checked every time the radio is serviced. The frequency counter used for this procedure must have a stability of 0.1 ppm (or better).

1. From the Service menu, select Tx Alignment.
2. Select Reference Oscillator to open the reference oscillator tuning window.
3. Press Toggle PTT to key the radio. The status bar will indicate that the radio is transmitting.
4. Measure the transmit frequency on your frequency counter.
5. Adjust the reference oscillator softpot on the RSS screen to achieve a frequency as measured on the frequency counter to be within the limits shown in table 6.2-2 of the target frequency displayed on the RSS window.
6. Press Toggle PTT again to dekey the radio and then press Program to store the softpot value.

Table 6.2-2 Reference Oscillator Alignment.

RF-Band	Target
300-345MHz	±150 Hz

1.6 Front-End Pre-Selector

Alignment of the front-end pre-selector is normally not required on these radios. Only if the radio has poor receiver sensitivity or the pre-selector parts have been replaced the following procedure should be performed. The softpot value sets the control voltage of the pre-selector. Its value needs to be set at 7 frequencies across the frequency range.

1. Set the test box (GTF180) meter selection switch to the “Audio PA” position and connect a SINAD meter to the “METER” port.
2. From the Service menu, select Rx Alignment.
3. Select Front End Filter to open the pre-selector tuning window. The window will indicate the receive test frequencies to be used.
4. Select the first test frequency shown, and set the corresponding value to the start value shown in Table 6.2-3.
5. Set the RF test generator to the receive test frequency, and set the RF level to 10µV modulated with a 1kHz tone at the normal test deviation shown in table 6.2-4.
6. Measure the RSSI voltage at accessory connector pin 15 with a dc voltmeter capable of 1 mV resolution. The RSSI output is available on A2, 4 channel, radios but it is unbuffered. Therefore a high impedance (1 MΩ) voltmeter must be used.
7. Decrease the softpot value and note the RSSI voltage. The target softpot value is achieved when the voltage change between 2 softpot steps is lower than 0.75% of the RSSI voltage for the first time. Set test box (GTF180) audio switch to the “SPKR” position. The 1kHz tone must be audible at the target value to make sure the radio is receiving.
8. Repeat steps 4 - 7 for all test frequencies shown in the window.
9. Press Program to store the softpot values.

Table 6.2-3 Start Value for Front-End Pre-selector Tuning.

RF-Band	Start Value
300-345MHz	Maximum

Table 6.2-4 Normal Test Deviation.

Channel Spacing	Deviation
12.5 kHz 20 kHz 25 kHz	1.5 kHz 2.4 kHz 3 kHz

1.7 Rated Volume

The rated volume softpot sets the volume at normal test modulation.

1. Set test box (GTF180) meter selection switch to the “AUDIO PA” position and the speaker load switch to the “MAXAR” position. Connect an AC voltmeter to the test box meter port.
2. From the Service menu, select Rx Alignment.
3. Select Rated Volume to open the rated volume tuning window. The screen will indicate the receive test frequency to be used.
4. Set the RF test generator to the receive test frequency, and set the RF level to 1mVolt modulated with a 1kHz tone at the normal test deviation shown in table 6.2-4. Set test box (GTF180) audio switch to the “SPKR” position. The 1kHz tone must be audible to make sure the radio is receiving.
5. Adjust the value of the softpot to obtain rated audio volume (as close to 3.74 Vrms)
   Note: The voltage at the meter port of the testbox GTF180 is only half the voltage at the speaker.
6. Press Program to store the softpot value.

1.8 Squelch

The squelch softpots set the signal to noise ratio at which the squelch opens. The squelch value needs to be set at 7 frequencies across the frequency range. For 20/25kHz radios, the radio stores separate tuning data for 20kHz and 25kHz channel spacing. Therefore, both sets of tuning data should be set independently.

1. Set the test box (GTF180) meter selection switch to the “Audio PA” position and connect a SINAD meter to the “METER” port.
2. From the Service menu, select Rx Alignment.
3. Select ‘Squelch’ to open the squelch tuning window. This window is used to set the values for 12.5kHz radios and the 25kHz data for 20/25kHz radios. The window will indicate the receive test frequencies to be used.
4. Select the first test frequency shown, and set the corresponding value to 0.
5. Set the RF test generator to the test frequency and modulate the signal generator at the normal test deviation shown in table 6.2-4, with 1kHz tone. Adjust the generator for a 8-10 dB SINAD level (weighted with psophometric filter).
6. Adjust the softpot value until the squelch just closes.

7. Monitor for squelch chatter; if chatter is present, repeat step 6.
8. When no chatter is detected, select the next softpot and repeat steps 4 - 7 for all test frequencies shown in the window.
9. Press Program to store the softpot values.
10. If the radio is a 20/25kHz channel spacing model, repeat steps 1-9 for 20kHz channel spacing using the ‘Squelch (20kHz)’ window.

1.9 Transmit Deviation Limit

The transmit deviation limit softpot sets the maximum deviation of the carrier. Unlike other radios, the deviation limit for GM350 is set using low frequency (PL) rather than the usual 1kHz tone. The deviation value needs to be set at 7 frequencies across the frequency range. No audio signals need to be injected, as the radio generates a 82.5Hz tone while the deviation limit alignment window is open. This tone is used to set the maximum deviation. For 20/25kHz radios, the radio stores separate tuning data for 20kHz and 25kHz channel spacing. Therefore, both sets of tuning data should be set independently.

1. From the Service menu, select Tx Alignment.
2. Select ‘Deviation Limit’ to open the deviation limit tuning window. This window is used to set the values for 12.5kHz radios and the 25kHz data for 20/25kHz radios. The window will indicate the transmit test frequencies to be used.
3. Select the first test frequency shown in the window.
4. Press Toggle PTT to key the radio. The status bar will indicate that the radio is transmitting.
5. Adjust the transmitter deviation to the value shown in table 6.2-5.
6. Press Toggle PTT to dekey the radio.
7. Repeat steps 3- 6 for the remaining test frequencies.
8. Press Program to store the softpot values.
9. If the radio is a 20/25kHz channel spacing model, repeat steps 1 - 8 for 20kHz channel spacing using the ‘Deviation Limit (20kHz)’ window.

Table 6.2-5 Transmitter Deviation Limit Alignment Target.

Channel Spacing	Deviation
12.5 kHz	375 Hz
20 kHz	600 Hz
25 kHz	750 Hz

1.10 Transmit Modulation Balance (Compensation)

Compensation alignment balances the modulation sensitivity of the VCO and reference modulation (synthesizer low frequency port) lines. Compensation algorithm is critical to the operation of signalling schemes that have very low frequency components (e.g. PL) and could result in distorted waveforms if improperly adjusted. The compensation value needs to be set at 7 frequencies across the frequency range. For 20/25kHz radios, the radio stores separate tuning data for 20kHz and 25kHz channel spacing. Therefore, both sets of tuning data should be set independently.

1. From the Service menu, select Tx Alignment.
2. Select 'Modulation Balance' to open the deviation balance tuning window. This window is used to set the values for 12.5kHz radios and the 25kHz data for 20/25kHz radios. The window will indicate the transmit test frequencies to be used.
3. Set the Test Box (GTF180) meter selector switch to the "GEN" position, and inject a 2kHz (two kilohertz) tone at 800 mVrms (eight-hundred millivolts) into the "Audio In" port.
4. Connect an AC meter to the meter port to insure the proper input signal level.
5. Select the first test frequency shown in the window.
6. Press Toggle PTT to key the radio. The status bar will indicate that the radio is transmitting.
7. Measure the transmitter deviation.
8. Adjust the transmitter deviation using the appropriate softpot to the value shown in Table 6.2-6.
9. Press Toggle PTT to dekey the radio.
10. Repeat steps 5- 9 for the remaining test frequencies.
11. Press Program to store the softpot values.
12. If the radio is a 20/25kHz channel spacing model, repeat steps 1 - 11 for 20kHz channel spacing using the 'Modulation Balance (20kHz)' window.

Table 6.2-6 Transmitter Deviation.

Channel Spacing	Deviation
12.5 kHz	2.1-2.2 kHz
20 kHz	3.4-3.5 kHz
25 kHz	4.3-4.5 kHz

Chapter 6.3

Theory of Operation

Table of Contents

Paragraph		Page
1.0	**Overview**	1
2.0	**Controller**	2
2.1	General	2
2.2	Voltage Regulators	2
2.3	Electronic On/Off	3
2.4	Mechanical On/Off	3
2.5	Ignition	3
2.6	Hook	4
2.7	Microprocessor Clock Synthesizer	4
2.8	Serial Peripheral Interface (SPI)	4
2.9	SPEB Serial Interface	5
2.10	General Purpose Input/Output	5
2.11	Normal Microprocessor Operation	5
2.12	Control Head Model A2 or A3	6
	Controller Board Audio and Signalling Circuits	
3.0	**General**	7
3.1	Audio Filter IC (AFIC)	7
3.2	Audio Ground	7
4.0	**Transmit Audio Circuits**	7
4.1	Mic Input Path	7
4.2	External Mic Path	8
4.3	PTT Sensing and TX Audio Processing	8
4.4	Option Board Audio (128ch only)	9

Paragraph Page

5.0 Transmit Signalling Circuits 10
5.1 Sub-audible Data (PL/DPL) 10
5.2 High Speed Data and DTMF 11

6.0 Receive Audio Circuits 12
6.1 Squelch Detect 12
6.2 Audio Processing and Digital Volume Control 13
6.3 Audio Amplification Speaker (+) Speaker (-) 13
6.4 Handset Audio 14
6.5 Filtered Audio 14
6.6 Discriminator Audio (Unfiltered) 14
6.7 Option Board Audio 14

7.0 Receive Signalling Circuits 15
7.1 Sub-audible Data Decoder (PL/DPL) 15
7.2 High Speed Data Decoder 15
7.3 Alert Tone Circuits 16

300MHz Specific Circuit Description

8.0 Receiver Front-End 17
8.1 Front-End Band-Pass Filter and Pre-Amplifier 17
8.2 Mixer and Intermediate Frequency (IF) Section 17
8.3 IF IC (U5201) 18

9.0 Power Amplifier (PA) 5-25W 18
9.1 Power Controlled Stage 18
9.2 PA Stages 19
9.3 Directional Coupler 19
9.4 Antenna Switch 19
9.5 Harmonic Filter 20
9.6 Power Control 20

10.0 Frequency Synthesis 21
10.1 Reference Oscillator 21
10.2 Fractional-N Synthesizer (U8701) 21
10.3 Voltage Controlled Oscillator (VCO) 22
10.4 Synthesizer Operation 22

1.0 Overview

This section provides a detailed theory of operation for the radio and its components.

The main radio is designed to accept one additional option board. This may provide functions such as secure voice/or a signalling decoder.

The control head is mounted directly on the front of the radio. The control head contains a speaker, LED indicators, a microphone connector, buttons and dependant of radio type, a display. These provide the user with interface control over the various features of the radio.

In addition to the power cable and antenna cable, an accessory cable can be attached to a connector on the rear of the radio. The accessory cable provides the necessary connections for items such as external speaker, foot operated PTT, ignition sensing, etc.

2.0 Controller

2.1 General

The radio controller consists of 4 main subsections:

- ☐ Digital Control
- ☐ Audio Processing
- ☐ Power Control
- ☐ Voltage Regulation

The digital control section of the radio board is based upon a closed architecture controller configuration.

The digital section consists of a microprocessor, support memory, support logic, signal MUX ICs, the On/Off circuit, and general purpose Input/Output circuitry.

The closed architecture controller uses the Motorola 68HC11E9 (U0101) for a 4 channel radio and the 68HC11E20 for a 128 channel radio. In this configuration RAM and ROM are contained within the microprocessor itself. The only external memory device in the closed architecture controller is an EEPROM (2KByte for 128 channel radio).

Note: From this point on the 68HC11E9 or E20 microprocessor will be referred to as E9/20μP or μP. References to a Control Head will be to radio model A3 (Display radio).

2.2 Voltage Regulators

Voltage regulation for the controller is provided by 3 separate devices; U0631 (LP2951CM) +5V, U0601 (LM2941T) +9.3V, and UNSW 5V (a combination of R0621 and VR0621). An additional regulator is located in the RF section.

Voltage regulation providing 5V for the digital circuitry is done by U0631. Input and output capacitors (C0631/0632 and C0633-0635) are used to reduce high frequency noise and provide proper operation during battery transients. This regulator provides a reset output (pin 5) that goes to 0 volts if the regulator output goes out of regulation. This is used to reset the controller to prevent improper operation. Diode D0631 prevents discharge of C0632 by negative spikes on the 9V3 voltage

Regulator U0601 is used to generate the 9.3 volts required by some audio circuits, the RF circuitry and power control circuitry. Input and output capacitors (C0601-0603 and C0604/0605) are used to reduce high frequency noise. R0602/R0603 sets the output voltage of the regulator. If the voltage at pin 1 is greater than 1.3 volts the regulator output decreases and if the voltage is less than 1.3 volts the regulator output increases. This regulator output is electronically disabled by a 0 volt signal on pin 2. Q0601 and associated circuitry (R0601/0604/0605 and C0606) are used to disable the regulator when the radio is turned off.

UNSW 5V is only used in a few areas which draw low current and requires 5 V while the radio is off.

UNSW 5V CL is used to buffer the internal RAM. C0622 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Diode D0621 prevents radio circuitry from discharging this capacitor.

The voltage 9V3 SUPP is only used in the VHF radio to supply the drain current for the RF MOS FET in the PA.

The voltage SW B+ is monitored by the µP through the voltage divider R0641/R0642. Diode VR0641 limits the divided voltage to 5.1V to protect the µP.

Diode D5601 (UHF) / D3601 (VHF) located on the PA section acts as protection against transients and wrong polarity of the supply voltage.

2.3 Electronic On/Off

The radio has circuitry which allows radio software and/or external triggers to turn the radio on or off without direct user action. For example, automatic turn on when ignition is sensed and off when ignition is off.

Q0611 is used to provide SW B+ to the various radio circuits. Q0611 acts as an electronic on/off switch controlled by Q0612. The switch is on when the collector of Q0612 is low. When the radio is off Q0612 is cutoff and the voltage at Q0611-base is at A+. This effectively prevents current flow through Q0611 from emitter to collector. When the radio is turned on the voltage at the base of Q0612 is high (about 0.6V) and Q0612 switches on (saturation) and pulls down the voltage at Q0611-base. With Transistor Q0611 now enabled current flows through the device. This path has a very low impedance (less than 1 ohm) from emitter to collector. This effectively provides the same voltage level at SWB+ as at A+.

The electronic on/off circuitry can be enabled by the microprocessor (through AFIC port GCB1, line B+ CONTROL), the mechanical On/Off button on the control head (line ON OFF CONTROL), or the ignition sense circuitry (line IGNITION CONTROL). If any of the 3 paths cause a low at the collector of Q0612, the electronic ON is engaged.

2.4 Mechanical On/Off

This refers to the on/off button, located on the control head, and which turns the radio on and off. If the radio is turned off and the on/off button is pressed, line ON OFF CONTROL goes high and switches the radio on as long as the button is pressed. The microprocessor is alerted through line ANALOG 3 which is pulled to low by Q0925 (Control Head Model A3) while the on/off button is pressed. If the software detects a low state it asserts B+ CONTROL via AFIC pin 39 low which keeps Q0612 and Q0611, and in turn the radio switched on.

If the on/off button is pressed and held while the radio is on, the software detects the line ANALOG 3 changing to low and switches the radio off by setting B+ CONTROL to low.

2.5 Ignition

Ignition sense is used to prevent the radio from draining the vehicle's battery because the engine is not running.

When the IGNITION input (J0400- 10) goes above 6 volts Q0421 and Q0612 turn on. This turns on SW B+ by turning on Q0611 via line IGNITION CONTROL and Q0612 and the microprocessor starts execution. The software reads the line IGNITION SENSE, determines from the level that the IGNITION input is active and sets the B+ CONTROL output of the AFIC pin 39 to high to latch on SW B+.

When the IGNITION input goes below 6 volts, Q0421 switches off and R0426, R0427 pull line IGNITION SENSE high. The software is alerted by line IGNITION SENSE to switch off the radio by setting B+ CONTROL to low. The next time the IGNITION input goes above 6 volts the above process will be repeated.

2.6 Hook

The HOOK input is used to inform the µP when the Microphone´s hang-up switch is engaged. The signal is routed from J0101-3 and transistor Q0137 to the E9/20µP U0101-56. The voltage range of HOOK in normal operating mode is 0-5V. If a rear GP input line is set as HOOK then the front HOOK signal is overriden.

2.7 Microprocessor Clock Synthesizer

The controller uses the oscillator in the microprocessor E9/20µP along with some external components (C0115-C0117, L0114, R0115, Y0114) to generate the clock. Q0114 is used to alter the clock frequency slightly under software control if there is a possibility of harmonics of this clock source interfering with the desired radio receive frequency.

2.8 Serial Peripheral Interface (SPI)

The µP communicates to many of the IC's through its SPI port. This port consists of SPI TRANSMIT DATA (MOSI) (E9/20µP:U0101-52), SPI RECEIVE DATA (MISO) (E9/20µP:U0101-51), SPI CLK (E9/20µP:U0101-53) and chip select lines going to the various IC's, connected on the SPI PORT (BUS). This BUS is a synchronous bus, in that the timing clock signal CLK is sent while SPI data (SPI TRANSMIT DATA or SPI RECEIVE DATA) is sent. Therefore, whenever there is activity on either SPI TRANSMIT DATA or SPI RECEIVE DATA there should be a uniform signal on CLK. The SPI TRANSMIT DATA is used to send serial from a µP to a device, and SPI RECEIVE DATA is used to send data from a device to a µP. The only device from which data can be received via SPI RECEIVE DATA is the EEPROM (U0108)

On the controller there are three ICs on the SPI BUS, AFIC (U103-33), EEPROM (U0108-1) and D/A (U0731-6). In the RF sections there is one IC on the SPI BUS, the FRAC-N Synthesizer. The SPI TRANSMIT DATA and CLK lines going to the RF section are filtered by L0194/L0195 to minimize noise. The chip select lines for the IC´s are decoded by the address decoder U102.

The SPI BUS is also used for the control head. U0104-1,2 buffer the SPI TRANSMIT DATA and CLK lines to the control head. U0104-3 switches off the CLK signal for the LCD display if it is not selected via LCD CE.

When the µP needs to program any of these IC's it brings the chip select line for that IC to a logic 0 and then sends the proper data and clock signals. The amount of data sent to the various IC's are different, for example the FRAC-N can receive up to 13 bytes (97 bits) while the DAC can receive up to 3 bytes (24 bits). After the data has been sent the chip select line is returned to a logic 1.

The Option board interfaces are different in that the µP can also read data back from devices connected.

The timing and operation of this interface is specific to the option connected, but generally follows the pattern:

1) an option board device generates the interrupt,
2) main board asserts a chip select for that option board device,
3) the main board μP generates the CLK, and
4) when data transfer is complete the main board terminates the chip select and CLK activity.

2.9 SPEB Serial Interface

The SBEP serial interface allows the radio to communicate with the Radio Service Software (RSS). This interface connects to the Microphone connector (J0903/J0803) via Control Head connector (J0101) and comprises BUS+ (J0101-15). The line is bi-directional, meaning that either the radio or the RSS can drive the line.

When the RSS needs to communicate with the radio, an interrupt is generated by the BUS+ signal through R0104. The μP then starts serial data communication on BUS+ by sending data from pin 50 through D0101 and receiving data at pin 47 through R0104. While the radio is sending serial data at pin 50 it receives an ”echo” of the same data at pin 47.

2.10 General Purpose Input/Output

The Controller provides six general purpose lines (GP1 through GP6) available on the accessory connector J0400 to interface to external options. Lines GP1,4 are inputs, GP2 is an output and GP3,5,6 are bidirectional. The software and the hardware configuration of the radio model define the function of each port. Some ports are not connected on the 4ch radio, refer to appendix B.

GP1 can be used as external PTT input or others, set by the RSS.

GP2 can be used as normal output (Q0441 placed) or external alarm output (Q0442 placed). The voltage range can be set by R0442 (0-5V) or R0443 (0 - supply voltage).

GP4 can be used as normal input (D0471, R0477 not placed) or emergency input (D0471, R0477 placed).

GP3,5,6 are bidirectional and use the same circuit configuration. Each port uses an output transistor controlled by μP port PB5,4,7 and an input transistor read by μP port PC2,5,3. To use one of the GP´s as input the μP must turn off the corresponding output transistor.

In addition the signals from GP3-6 are fed to the option board connectors J0102, J0103.

The 470pF and 10nF capacitors serve to filter out any AC noise which may ride on the GP lines.

2.11 Normal Microprocessor Operation

The E9/20μP (U0101) contains internal 12 (E9) or 20 (E20) Kilobytes ROM, 512 (E9) or 768 (E20) bytes SRAM and 512 bytes EEPROM.

The E9/20μP RAM is always powered to maintain parameters such as the last operating mode. This is achieved by maintaining 5V at U0101-25. Under normal conditions, when the radio is off UNSW +5V is formed by FLT A+ running to D0621.

C0622 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Diode D0621 prevents radio circuitry from discharging this capacitor.

U0101-22 is the high reference voltage for the A/D ports on the E9/20µP. Resistor R0105 and capacitor C0105 filter the +5V reference. If this voltage is lower than +5V the A/D readings will be incorrect. Likewise U0101-21 is the low reference for the A/D ports. This line is normally tied to ground. If this line is not connected to ground, the A/D readings will be incorrect.

The MODB (U0101-25) input of the E9/20µP must be at a logic 1 for it to start executing correctly. The XIRQ (U0101-45) and the IRQ (U0101-46) pins should also be at a logic 1.

Optional external EEPROM (U0108) is available on some radio models. The external EEPROM is accessed through a serial connection. The E9/20µP generates SPI CLK (U0101-53), SPI TRANSMIT DATA (MOSI) (U0101-52) and SPI RECEIVE DATA (MISO) (U0101-51) to read or write EEPROM. On a read of EEPROM the E9/20µP continues generating the clock and the EEPROM places the requested data on the SPI RECEIVE DATA (MISO) line. On a write the message is followed by the data to be written to the EEPROM.

2.12 Control Head Model A2 or A3

Two Control Head versions (A2 or A3) are available for user interface. Both Control Heads contain the internal speaker, the microphone connector, several buttons to operate the radio and several indicator LEDs to inform the user about the radio status. Additionally the Control Head model A3 uses a 3 digit, 7 segment, LCD display for the channel number.

The On/Off button when pressed switches the voltage regulators on by pulling ON OFF CONTROL to high and connects the base of Q0925(A3), Q0825(A2) to FLT A+. This transistor pulls the line ANALOG 3 to low to inform the µP that the On/Off button is pressed. If the radio is switched off, the µP will switch it on and vice versa. All other buttons work the same way. If a button is pressed, it will connect one of the 3 lines ANALOG 1,2,3 to a resistive voltage divider connected to +5V. The voltages of the lines are A/D converted inside the µP and specify the pressed button.

All the back light and indicator LEDs are driven by current sources and controlled by the µP via SERIAL PERIPHERAL INTERFACE (SPI) interface. The LED status is stored in shiftregister U0941(A3), U0841(A2). Line LED CE enables the serial write process via Q0941(A3), Q0841(A2) while line LED CLCK BUF shifts the data of line SPI DATA BUF into the shiftregister.

In addition Control Head Model A3 contains the LCD display H0931. The display data of line SPI DATA BUF is shifted into the display driver by clock signal LCD CLCK BUF.

CONTROLLER BOARD AUDIO AND SIGNALLING CIRCUITS

3.0 General

3.1 Audio Filter IC (AFIC)

The AFIC (U0103) used in the controller performs RX/TX audio shaping, i.e. filtering, amplification, attenuation.

The AFIC is programmable through the SPI BUS (U0103-30/31/33), normally receiving 6 bytes. This programming sets up various paths within the AFIC to route audio signals through the appropriate filtering, gain and attenuator blocks. The AFIC also has 4 General Control Bits GCB1,3-5 which are CMOS level outputs. GCB1 is used to switch the radio on and off under µP control via line B+ CONTROL. GCB3 is used to switch the audio PA on and off (AUDIO PA ENABLE). GCB4 selects between the UNATTEN RX OUT audio signal and the unfiltered DET AUDIO signal. GCB5 HIGH LOW BAND can be used to switch between band splits.

3.2 Audio Ground

VAG is the dc bias used as an audio ground for the op-amps that are external to the Audio Filter IC (AFIC). U0105-1 forms this bias by dividing 9.3V with resistors R0171, R0172 and buffering the 4.65V result with a voltage follower. VAG emerges at pin 1 of U0105-1. C0172 is a bypass capacitor for VAG. The AFIC generates its own 2.5 V bias for its internal circuitry. C0153 is the bypass for the AFIC's audio ground dc bias. Note that while there are AFIC VAG, and BOARD VAG (U0105-1) each of these are separate. They do not connect together.

4.0 Transmit Audio Circuits

Refer to Figure 6.3-1 for reference for the following sections.

4.1 Mic Input Path

The radio supports 2 distinct microphone paths known as internal and external mic and an auxiliary path (FLAT TX AUDIO). The microphones used for the radio require a DC biasing voltage provided by a resistive network.

These two microphone audio inputs are connected together. Following the internal mic path; the microphone is plugged into the radio control head and is connected to the controller board via J0101-16. From here the signal is routed to C0142. R0141 and R0142 provide the 9.3VDC bias. R0142 and C0141 provide a 1kΩ AC path to ground that sets the input impedance for the microphone and determines the gain based on the emitter resistor in the microphone's amplifier circuit.

The MIC signal is routed to the AFIC´s TX IN input (U0103-10) through R0146 and R0145 (4 channel radio) or through op-amp buffer U0106-2 and option board connector J0103-3,1 (128 channel radio). The audio signal at the output of U0106-2 should be approximately 80mV deviation with 25kHz channel spacing.

The FLAT TX AUDIO signal from accessory connector U0400-5 is buffered by op-amp U0106-1 and fed to the AFIC U0103-13 through gate U0107-1. Gate U0107-1 is controlled by the μP port PC7 (U0101-42) and selects between FLAT TX AUDIO or signalling signal created by the μP.

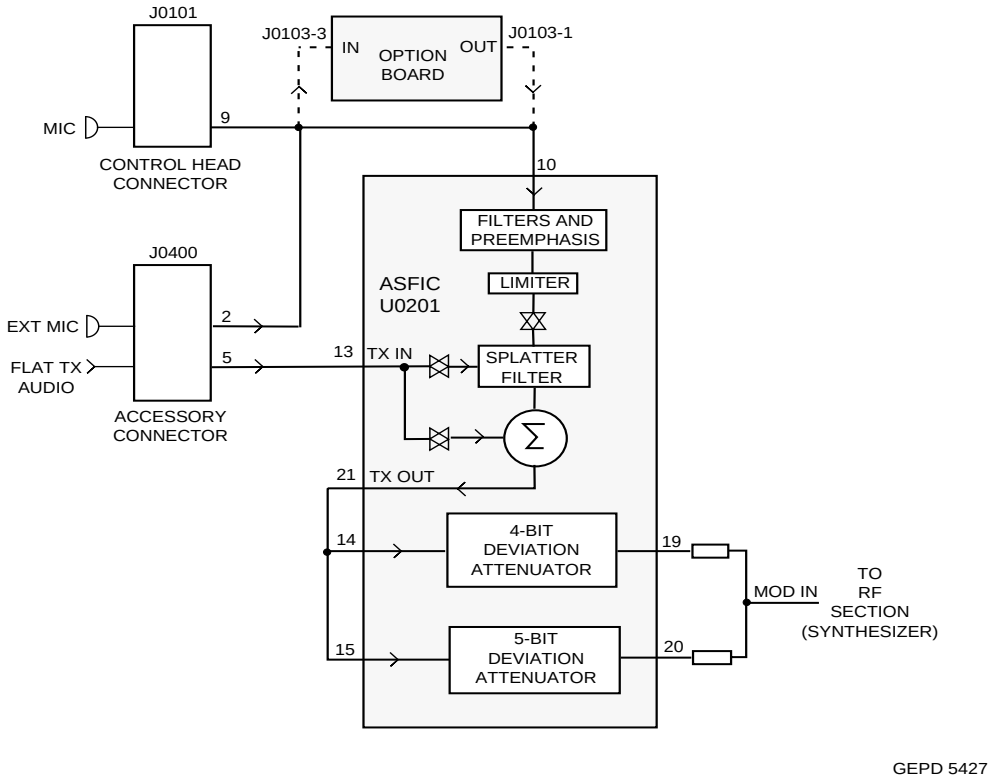


Figure 6.3-1 Transmit Audio Paths

4.2 External Mic Path

The external microphone signal enters the radio on accessory connector J0400 pin 2 and connects to the standard microphone input through R0421.

4.3 PTT Sensing and TX Audio Processing

Mic PTT is sensed by the μP U0101 pin 22. An external PTT can be generated by grounding pin 3 on the accessory connector if this input is programmed for PTT.

The MIC signal is routed to the AFIC (U0103) through R0146 and R0145 (4 channel radio) or through op-amp buffer U0106-2 and option board connector J0103-3,1 (128 channel radio). R0145, C0145, the amplifier inside the AFIC (pins 9,10) and gain setting resistor R0147 pre-emphasise the MIC audio signal. After further limiting and filtering the modulation signal emerges from the AFIC at U0103-19/20. Both signals are weighted by resistors R0181, R0182 and add up to signal MOD IN.

4.4 Option Board Audio (128ch only)

The audio coming from the microphone (J0101-16) or the external microphone (J0400-2) is routed through op-amp buffer U0106-2 (128ch only) to the option board connector J0103-3. After option board processing the signal emerges at J0103-1. The source resistor of the option board output and C0145, the amplifier inside the AFIC (U0103-9,10) and gain setting resistor R0147 pre-emphasise the signal. Inside the AFIC the signal follows a path identical to conventional transmit audio. The modulation signal emerges from the AFIC at J0103-19/20. Both signals are weighted by resistors R0181, R0182 and add up to signal MOD IN.

5.0 Transmit Signalling Circuits

Refer to Figure 6.3-2 for reference for the following sections. From a hardware point of view, there are three types of signalling:

1. Sub-audible data (PL / DPL / Connect Tone) that gets summed with transmit voice or signalling,
2. DTMF data for telephone communication in trunked and conventional systems, and
3. Audible signalling including Select 5, MPT-1327, MDC, Single Tones.

All three types are supported by the hardware while the radio software determines which signalling type is available. Currently only PL/DPL and Single tones are supported in the software.

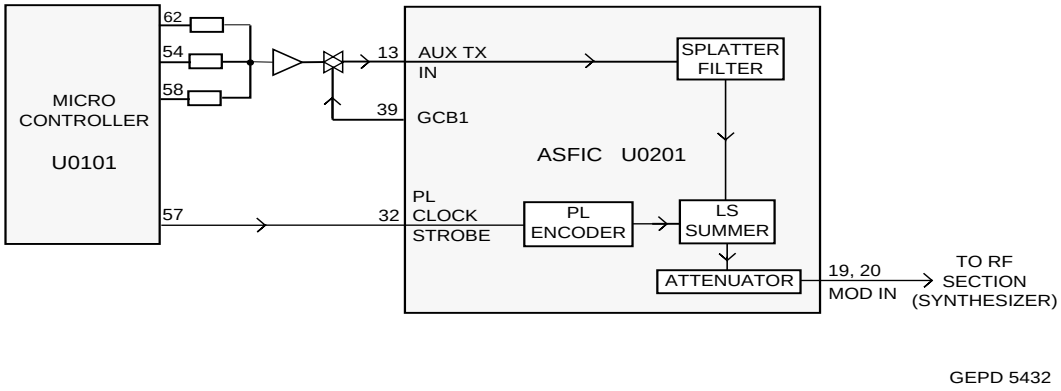


Figure 6.3-2 Transmit Signalling Paths

5.1 Sub-audible Data (PL/DPL)

Sub-audible data implies signalling whose frequency is below 300Hz. Although it is referred to as ”sub-audible data,” the actual frequency spectrum of these waveforms may be as high as 250 Hz, which is audible to the human ear. However, the radio receiver filters out any audio below 300Hz, so these tones are never heard in the actual system.

Only one type of sub-audible data can be generated by U0103 (AFIC) at any one time. The process is as follows, using the SPI BUS, the μP programs the AFIC to set up the proper low-speed data deviation and select the PL or DPL filters. The μP then generates a square wave which strobes the AFIC PL / DPL encode input PL CLOCK STROBE U0103-32 at twelve times the desired data rate. For example, for a PL frequency of 103Hz, the frequency of the square wave would be 1236Hz.

This drives a tone generator inside U0103 which generates a staircase approximation to a PL sine wave or DPL data pattern. This internal waveform is then low-pass filtered and summed with voice or data. The resulting summed waveform then appears on U0103-19,20 (MOD IN), where it is sent to the RF board as previously described for transmit audio.

5.2 High Speed Data and DTMF

The High Speed Data and DTMF waveforms are created by the μP U0101 using summer U0105-3. Op-amp U0105-3 and resistors R0121-R0124 add up the three signals coming from the μP pins 58, 59 and 62. The output signal of U0105-3 is routed to the AFIC (U0103-13) through gate U0107-1. Inside the AFIC the signal enters the conventional transmitter audio path at the splatter filter input. Gate U0107-1 controlled by μP port PC7 (U0101-42) selects between data signal and FLAT TX AUDIO signal. Microphone audio is muted during High Speed Data signalling.

6.0 Receive Audio Circuits

Refer to Figure 6.3-3 for reference for the following sections.

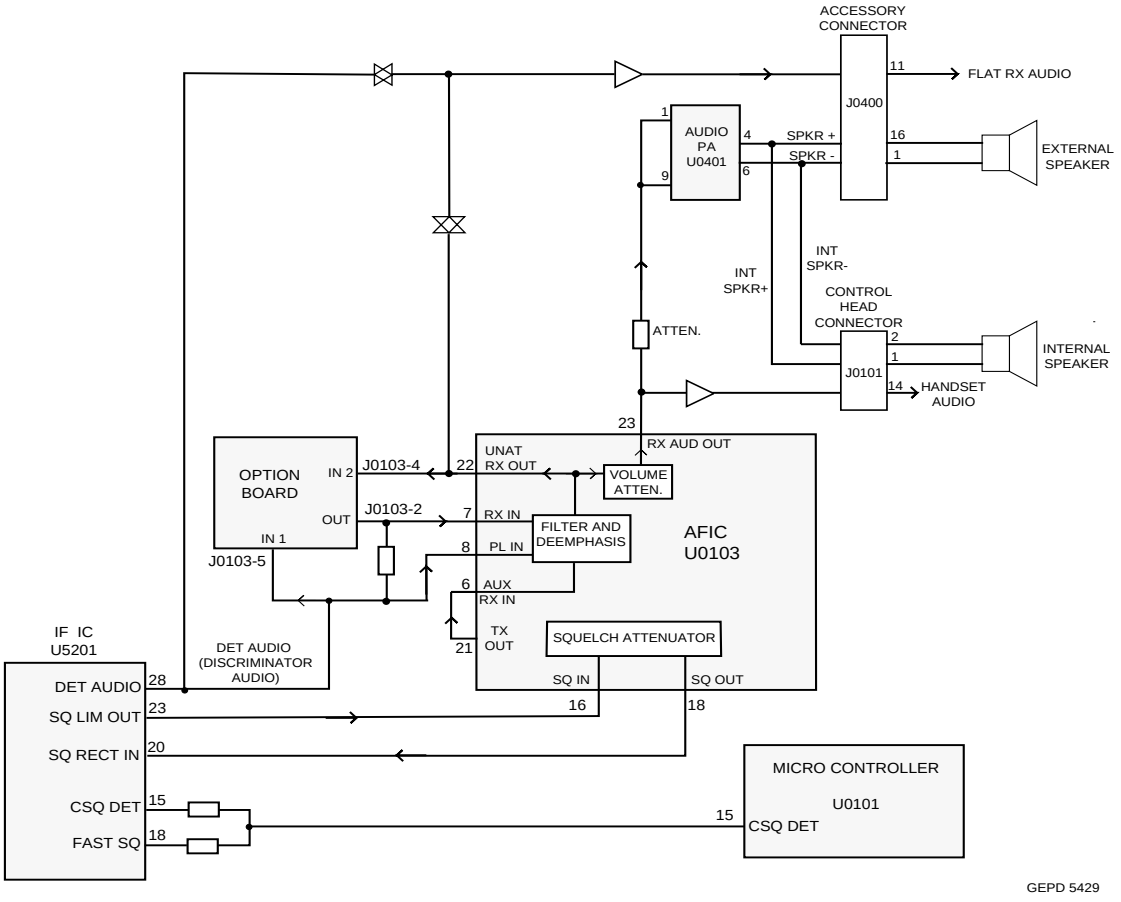


Figure 6.3-3 Receive Audio Paths.

6.1 Squelch Detect

The IF IC controls the squelch characteristics of the radio. With a few external parts (R5521, R5222, C5225, C5226, C5229, C5230, R5223) the squelch tail, hysteresis, attack and delay are optimized for the radio. To set the squelch threshold the signal from IF IC pin 23 (line SQ ATT IN) is routed to the squelch attenuator input of the AFIC (U0103-16). The attenuated signal (line SQ ATT OUT) from the AFIC (U0103-18) enters the IF IC at pin 20 and is used to create a squelch indicator signal available at pin 15 (line CSQ DET).

The microprocessor controlled ADAPT signal at pin 22 activates the fast squelch indicator signal at IF IC pin 18 (FAST SQ). Both squelch indicator signals CSQ DET (pin 15) and FAST SQ (pin 18) are combined, weighted by resistors R0111 / R012 and fed to one of the microprocessor´s ADCs (U0101-15) for interpretation. From the voltage weighted by the resistors the µP determines whether CSQ DET, FAST SQ or both are active.

6.2 Audio Processing and Digital Volume Control

The receiver audio signal enters the controller section from the IF IC (U5201-28) on DET AUDIO. The signal is AC coupled by C0181 and enters the AFIC via the RX IN pin U0103-7.

Inside the AFIC the signal entering RX IN (U0103-7) goes through the audio path while the signal entering PL DPL IN (U0103-8) via C0182 goes through the PL/DPL path.

The audio path has a programmable amplifier, whose setting is based on the channel bandwidth being received, then a LPF filter to remove any frequency components above 3000Hz and then an HPF to remove any sub-audible data below 300Hz. Next, the recovered audio passes through a de-emphasis filter if it is enabled (to compensate for Pre-emphasis which is used to reduce the effects of FM noise). The IC then passes the audio through the 8-bit programmable attenuator whose level is set depending on the value of the volume control. Finally, the filtered audio signal passes through an output buffer within the AFIC. The audio signal exits the AFIC at RX AUDIO U0103-23.

The µP programs the attenuator, using the SPI BUS, based on the volume setting. The minimum/ maximum settings of the attenuator are set by codeplug parameters.

Since sub-audible signalling is summed with voice information on transmit, it must be separated from the voice information before processing. Any sub-audible signalling enters the AFIC from the IF IC at PL DPL IN U0103-8. Once inside it goes through the PL/DPL path. The signal first passes through one of 2 low pass filters, either PL low pass filter or DPL/LST low pass filter. Either signal is then filtered and goes through a limiter and exits the AFIC at PL DPL DECODER OUT U0103-27. At this point the signal will appear as a square wave version of the sub-audible signal which the radio received. The microprocessor (U0101-64) will decode the signal directly to determine if it is the tone/ code which is currently active on that mode.

6.3 Audio Amplification Speaker (+) Speaker (-)

The output of the AFIC´s digital volume pot, U0103-23 is routed through a voltage divider formed by R0401 and R0402 to set the correct input level to the audio PA (U0401). This is necessary because the gain of the audio PA is 46 dB, and the AFIC output is capable of overdriving the PA unless the maximum volume is limited.

The audio then passes through C0401 which provides AC coupling and low frequency roll-off. C0402 provides high frequency roll-off as the audio signal is routed to pins 1 and 9 of the audio power amplifier U0401.

The audio power amplifier has one inverted and one non-inverted output that produces the differential audio output SPK+ / SPK- (U0401-4/6). The inputs for each of these amplifiers are pins 1 and 9 respectively; these inputs are both tied to the received audio. The audio PA's DC biases are not activated until the audio PA is enabled at pin 8.

The audio PA is enabled via AUDIO PA ENABLE signal from the AFIC (U0103-40). When the base of Q0401 is low, the transistor is off and U0401-8 is high, using pull up resistor R0406, and the Audio PA is ON. The voltage at U0401-8 must be above 8.5VDC to properly enable the device. If the voltage is between 3.3 and 6.4V, the device will be active but has its input (U0401-1/9) off. R0404 ensures that the base of Q0401 is high on power up. Otherwise there may be an audio pop due to R0406 pulling U0401-8 high before the software can switch on Q0401.

The SPK+ and SPK- outputs of the audio PA have a DC bias which varies proportionately with FLT A+ (U0401-7). FLT A+ of 11V yields DC offset of 5V, and FLT A+ of 17V yields a DC offset of 8.5V. If either of these lines is shorted to ground, it is possible that the audio PA will be damaged. SPK+ and SPK- are routed to the accessory connector (J400-16 and 1) and to the control head (connector J0101-1 and 2).

6.4 Handset Audio

Certain hand held accessories have a speaker within them which require a different voltage level than that provided by U0401. For those devices HANDSET AUDIO is available at J0101-14.

The received audio from the output of the AFIC´s digital volume attenuator is also routed to U0105-4 pin 9 where it is amplified 15 dB; this is set by the 10k/68k combination of R0154 and R0155. This signal is routed from the output of the op amp U0105-4 pin 8 to J0101-14. The control head sends this signal directly out to the microphone jack. The maximum value of this output is 6.6Vp-p.

6.5 Filtered Audio

The AFIC has an audio whose output at U0103-22 has been filtered and de-emphasized, but has not gone through the digital volume attenuator. From AFIC U0103-22 the signal is routed through gate U0107-2 and AC coupled to U0106-4. The gate controlled by AFIC port GCB4 (U0103-2) selects between the filtered audio signal from the AFIC or the unfiltered discriminator signal from the IF IC U5201.The output at U0106-4 is then routed to J0400-11. Note that any volume adjustment of the signal on this path must be done by the accessory.

6.6 Discriminator Audio (Unfiltered)

Note that discriminator audio DET AUDIO from the IF IC U5201, in addition to being routed to the AFIC, is also routed to the option connector J0103-5 (See Secure Rx description blocks for further information).

6.7 Option Board Audio

Discriminator or filtered audio, enters the option board at connector J0103-5 and J0103-4. On the option board, the signal may be processed and then fed back through (J0103-2) to AUX RX IN of the AFIC (U0103-6). From then on it follows a path identical to conventional receive audio, where it is filtered (0.3 - 3kHz) and de-emphasized.

7.0 Receive Signalling Circuits

Refer to Figure 6.3-4 for reference for the following sections.

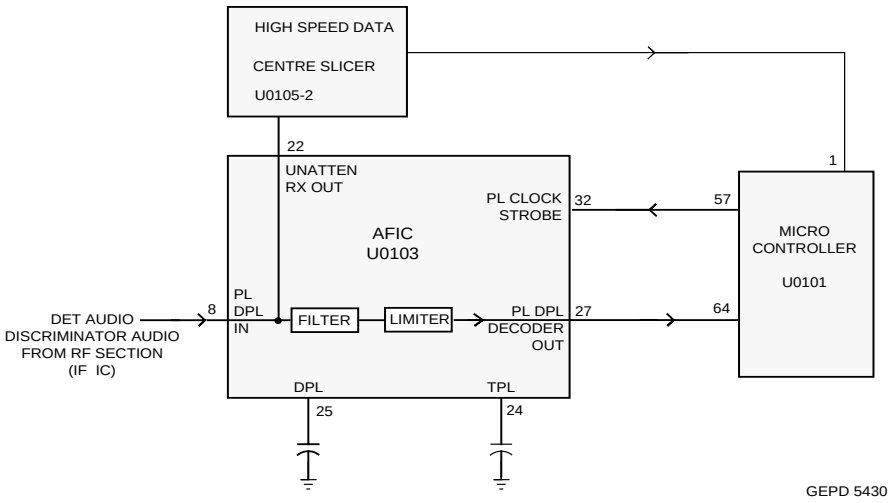


Figure 6.3-4 Receive Signalling Path.

7.1 Sub-audible Data Decoder (PL/DPL)

The receiver audio signal entering the AFIC U0103 at pin 8 first passes through the Tone PL filter or the Digital PL filter, depending on the PL option selected for the current operating mode. Filtered PL is then coupled to the PL detector circuit, with detected PL output at U0103-27. At this point the signal will appear as a square wave version of the sub-audible signal which the radio received. The microprocessor U0101-64 will decode the signal directly to determine if it is the tone / code which is currently active on that mode.

7.2 High Speed Data Decoder

The unattenuated receiver audio signal from U0103-22 is AC coupled to the input of centre slicer circuit U0105-2. The non-inverting input of op-amp U0105-2 is fed through resistor R0162. Capacitor C0164 sets a low-pass corner frequency of 3.3kHz. The inverting input of op-amp U0105-2 is fed through resistor R0163. Capacitor C0163 sets a low-pass corner frequency of 16Hz.

During operation, R0163 / C0163 establish an average DC offset level at U0105-2 pin 6 dependent on the average DC level of the undetected signal to set the “trigger” threshold of U0105-2. R0162 / C0164 provide high audio frequency roll-off to improve falsing immunity, but passes 600 or 1200 baud signals. The detected output from the centre slicer circuit is buffered and inverted by Q0161 and then coupled to the µP U0101-1 where algorithms perform the final decoding.

7.3 Alert Tone Circuits

When the software determines that it needs to give the operator an audible feedback (for a good key press, or for a bad key press), or radio status , it sends an alert tone to the speaker.

It does so by sending SPI BUS data to U0103 which sets up the audio path to the speaker for alert tones. The alert tone itself is generated by the AFIC.

The allowable internal alert tones are 410, 820, and 1640Hz. In this case a code contained within the SPI BUS load to the AFIC sets up the path and determines the tone frequency, and at what volume level to generate the tone. (It does not have to be related to the voice volume setting).

Inside the AFIC, this signal is routed to the alert tone generator; the output of the generator is summed into the audio chain just after the RX audio de-emphasis block. Inside U0103 the tone is amplified and filtered, then passed through the 8-bit digital volume attenuator, which is typically loaded with a special value for alert tone audio. The tone exits at U0103-23 and is routed to the audio PA like receive audio.

300-345MHz SPECIFIC CIRCUIT DESCRIPTION

8.0 Receiver Front-End

The receiver is able to cover the range from 300 to 350 MHz. It consists of four major blocks: front-end, mixer, first IF section and IF IC. Antenna signal pre-selection is performed by two varactor tuned bandpass filters. A double balanced schottky diode mixer converts the signal to the first IF at 45.1 MHz.

Two crystal filters in the first IF section and two ceramic filters in the second IF section provide the required selectivity. The second IF at 455 kHz is mixed, amplified and demodulated in the IF IC. The processing of the demodulated audio signal is performed by an audio processing IC located in the controller section.

8.1 Front-End Band-Pass Filter & Pre-Amplifier

A two pole pre-selector filter tuned by the varactor diodes D8301 and D8302 pre-selects the incoming signal (PA RX) from the antenna switch to reduce spurious effects to following stages. The tuning voltage (FE CNTL VLTG) ranging from 2 volts to 8 volts is controlled by a Digital to Analog (D/A) converter (U0731-11) in the controller section. A dual hot carrier diode (D8303) limits any inband signal to 0 dBm to prevent damage to the pre-amplifier.

The RF pre-amplifier is an SMD device (Q8301) with collector base feedback to stabilize gain, impedance, and intermodulation. The collector current of approximately 11-16 mA is drawn from the voltage 9V3 via L8302 and R8302.

A second two pole varactor tuned bandpass filter provides additional filtering to the amplified signal. The varactor diodes D8304 and D8305 are controlled by the same signal which controls the pre-selector filter. A following 1 dB pad (R8310, R8314, R8316) stabilizes the output impedance and intermodulation performance. If the radio is configured for a base station application, R8319 is not placed, and TP8301 and TP8302 are shorted.

8.2 Mixer and Intermediate Frequency (IF) Section

The signal coming from the front-end is converted to the first IF (45.1 MHz) using a double balanced schottky diode mixer (D8401). Its ports are matched for incoming RF signal conversion to the 45.1 MHz IF using low side injection. The injection signal (VCO MIXER) coming from the mixer buffer (Q8881) is filtered by the lowpass consisting of (L8403, L8404, C8401 - C8403) and has a level of approximately 10 dBm.

The mixer IF output signal (RX IF) from transformer T8401 pin 2 is fed to the first two pole crystal filter Y5201. The filter output in turn is matched to the following IF amplifier.

The IF amplifier Q5201 is actively biased by a collector base feedback (R5201, R5202) to a current drain of approximately 5 mA drawn from the voltage 5V STAB. Its output impedance is matched to the second two pole crystal filter Y5202. A dual hot carrier diode (D5201) limits the filter output voltage swing to reduce overdrive effects at RF input levels above -27 dBm.

8.3 IF IC (U5201)

The first IF signal from the crystal filters feeds the IF IC (U5201) at pin 6. Within the IF IC the 45.1MHz first IF signal mixes with the second local oscillator (LO) at 44.645MHz to the second IF at 455 kHz. The second LO uses the external crystal Y5211. The second IF signal is amplified and then filtered by two external ceramic filters (FL5201, FL5202). Back in the IF IC the signal is demodulated in a phase-lock detector and fed from IF IC pin 28 to the audio processing circuit AFIC U0103 located in the controller section (line DET AUDIO).

The IF IC also controls the squelch characteristics of the radio. With a few external parts (R5221, R5222, C5225, C5226, C5229, C5230, R5223) the squelch tail, hysteresis, attack and delay were optimized for the radio. To set the squelch threshold the signal from IF IC pin 23 (line SQ ATT IN) is attenuated by a microprocessor controlled audio processing IC AFIC (U0103) located in the controller section. The attenuated signal from the AFIC (line SQ ATT OUT) enters the IF IC at pin 20 and is used to create a squelch indicator signal available at pin 15 (CSQ DET).

The microprocessor controlled ADAPT signal at pin 22 activates the fast squelch indicator signal at IF IC pin 18 (FAST SQ). Both squelch indicator signals CSQ DET (pin 15) and FAST SQ (pin 18) are combined, weighted by R0111 / R0112 and fed to the microprocessor U0101 pin 15 for interpretation. From the voltage weighted by the resistors the uP determines whether CSQ DET, FAST SQ or both are active.

At IF IC pin 11 an RSSI signal is available with a dynamic range of 70 dB. The RSSI signal is buffered by op-amp U0106-3 and available at accessory connector J0400-15.

9.0 Transmitter Power Amplifier (PA) 5-25W

The transmitter is able to cover the range from 300 to 345 MHz.

The radio's 5-25 W PA is a four stage amplifier used to amplify the output from the exciter to the radio transmit level. It consists of four stages in the line-up. The first (Q8510) is a bipolar stage that is controlled via the PA control line. It is followed by another bipolar stage (Q8520), a MOS FET stage (Q8530, Q8531) and a final bipolar stage (Q8540). Devices Q8510, Q8520,Q8530 and Q8531 are surface mounted. Bipolar Transistor Q8540 is directly attached to the heat sink.

9.1 Power Controlled Stage

The first stage (Q8510) amplifies the rf signal from the VCO (line EXCITER PA) and controls the output power of the PA. The output power of the transistor Q8510 is proportional to its collector current which is adjusted by a voltage controlled current source consisting of Q8612 and Q8621. The whole stage operates off the K9V1 source which is 9.1V in transmit mode and nearly 0V in receive mode.

The collector current of Q8510 causes a voltage drop across the resistors R8623 and R8624. Transistor Q8612 adjusts the voltage drop across R8621 through PA control line (PWR CNTL). The current source Q8621 adjusts the collector current of Q8510 by modifying its base voltage until the voltage drop across R8623 and R8624 plus VBE (0.6V) equals the voltage drop across R8621 plus VBE (0.6V) of Q8611. If the voltage of PWR CNTL is raised, the base voltage of Q8612 will also rise causing more current to flow to the collector of Q8612 and a higher voltage drop across R8621. This in turn results in more current driven into the base of Q8510 by Q8621 so that the current of Q8510 is increased. The collector current settles when the voltage over the series configuration of R8623 and R8624 plus VBE of Q8621 equals the voltage over R8621 plus VBE (0.6V) of Q8611. By controlling the output power of Q8510 and in turn the input power of the following stages the ALC loop is able to regulate the output power of the transmitter. Q8611 is used for temperature compensation of the PA output power.

9.2 PA Stages

The bipolar transistor Q8520 is driven by Q8510. To reduce the collector-emitter voltage and in turn the power dissipation of Q8510 its collector current is drawn from the antenna switch circuit.

In transmit mode the base of Q8520 is slightly positive biased by a divided K9V1 signal. This bias along with the rf signal from Q8510 allows a collector current to be drawn from the antenna switch circuit and in turn switches the antenna switch to transmit, while in receive mode the low K9V1 signal with no rf signal present cuts off the collector current and in turn switches the antenna switch to receive.

The following stage uses two enhancement mode N-Channel MOS FET devices (Q8530, Q8531) and requires for each device a positive gate bias and a quiescent current flow for proper operation. The voltages of the lines BIAS VLTG and BIAS VLTG 2 are set in transmit mode by two Digital to Analog (D/A) converters (U0731-4, U0731-11) and fed to the gates of Q8531 and Q8530 via two resistive dividers. The bias voltages are tuned in the factory. If one or both transistor are replaced, the bias voltages must be tuned with the Service Software (RSS). Care must be taken, not to damage any device by exceeding the maximum allowed bias voltage. The collector currents are drawn from the supply voltage A+ via L8531 and L8532.

The final stage uses the bipolar device Q8540 and operates off the A+ supply voltage. For class C operation the base is DC grounded by two series inductors (L8533, L8534). A matching network consisting of C8541-C8544 and two striplines transform the impedance to 50 Ohms and feed the directional coupler.

9.3 Directional Coupler

The directional coupler is a microstrip printed circuit which couples a small amount of the forward power off the rf power from Q8541. The coupled signal is rectified to an output power proportional negative DC voltage by the diode D8553 and sent to the power control circuit in the controller section via the line PWR DETECT for output power control. The power control circuit holds this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

9.4 Antenna Switch

The antenna switch is switched synchronously with the K9V1 voltage and feeds either the antenna signal coming through the harmonic filter to the receiver or the transmitter signal coming from the PA to the antenna via the harmonic filter.

In transmit mode, this K9V1 voltage is high and biases Q8520 and, along with the rf signal from Q8510, allows a collector current to be drawn. The collector current of Q8520 drawn from A+ flows via L8542, L8541, directional coupler, D8551, L8551, D8631, L8631, R8616, R8617 and L8611 and switches the PIN diodes D8551 and D8631 to the low impedance state. D8551 leads the rf signal from the directional coupler to the harmonic filter. The low impedance of D8631 is transformed to a high impedance at the input of the harmonic filter by the resonant circuit formed by L8551, C8633 and the input capacitance of the harmonic filter.

In receive mode the low K9V1 and no rf signal present from Q8510 turn off the collector current of Q8520. With no current drawn by Q8520 and resistor R8615 pulling the voltage at PIN diode D8631 to A+ both PIN diodes are switched to the high impedance state. The antenna signal, coming through the harmonic filter, is channelled to the receiver via L8551, C8634 and line PA RX.

A high impedance resonant circuit formed by D8551 in off state and L8554, C8559 prevents an influence of the receive signal by the PA stages. The high impedance of D8631 in off state doesn´t influence the receiver signal.

9.5 Harmonic Filter

The transmitter signal from the antenna switch is channelled through the harmonic filter to the antenna connector J8501.The harmonic filter is formed by inductors L8552, L8553, and capacitors C8551 through C8554. This network forms a low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R8550 is used for electro-static protection.

9.6 Power Control

The power control loop regulates transmitter power with an automatic level control (ALC) loop and provides protection features against excessive control voltage and high operating temperatures.

MOS FET device bias, power and control voltage limit are adjusted under microprocessor control using a Digital to Analog (D/A) converter (U0731). The microprocessor writes the data into the D/A converter via serial interface (SRL) composed of the lines SPI CLCK SRC (clock), SPI DATA SRC (data) and DAC CE (chip enable). The D/A adjustable control voltage limit increases transmitter rise time and reduces adjacent channel splatter as it is adjusted closer to the actual operating control voltage.

The microprocessor controls K9V1 ENABLE (U0101-6) to switch on the first and the second PA stage via transistors Q0741, Q0742 and signal K9V1. The antenna switch is turned on by the collector current of the second PA stage. In TX mode the front-end control D/A (U0731-11) is used for BIAS VOLTAGE 2 (via R0736) and K9V1 ENABLE pulls signal FE CNTL VLTG to ground via Q0743. PA DISABLE, also microprocessor controlled (U0101-54), sets BIAS VLTG (U0731-4) and VLTG LIMIT SET (U0731-13) via D0731 and BIAS VLTG 2 via D0733 in receive mode to low to switch off the biases of the MOS FET devices Q8530, Q8531 and to switch off the power control voltage (PWR CNTL).

Through an Analog to Digital (A/D) input (VLTG LIMIT) the microprocessor can read the PA control voltage (PWR CNTL) during the tuning process.

The ALC loop regulates power by adjusting the PA control line PWR CNTL to keep the forward power voltage PWR DETECT at a constant level.

Opamp U0701-2 and resistors R0701 to R0703 and R0731 subtract the negative PWR DETECT voltage from the PA PWR SET D/A output U0731 pin 2. The result is connected to opamp inverting input U0701-4 pin 9 which is compared with a 4.6 volt reference VAG present at noninverting input U0701-4 pin 10 and controls the output power of the PA via pin 8 and control line PWR CNTL. The 4.6 volt reference VAG is set by a resistive divider circuit (R0171, R0172) which is connected to ground and 9.3 volts, and buffered by opamp U0105-1.

During normal transmitter operation the voltages at the opamp inputs U0701-4 pins 9 and 10 should be equal to 4.6 volts and the PA control voltage output at pin 8 should be between 4 and 7 volts. If power falls below the desired setting, PWR DETECT becomes less negative, causing the output at U0701-2 pin 7 to decrease and the opamp output U0701-4 pin 8 to increase.

A comparator formed by U0701-4 increases the PA control voltage PA CNTL until PWR DETECT is at the desired level. The power set D/A output voltage PA PWR SET (U0731-2) at U0701-2 pin 5 adjusts power in steps by adjusting the required value of PWR DETECT. As PA PWR SET (U0731-2) decreases, transmitter power must increase to make PWR DETECT more negative and keep the inverting input U0701-4 pin 9 at 4.6 volts.

Loop frequency response is controlled by opamp feedback components R0712 and C0711. Opamp U0701-3 compares the power control voltage PWR CNTL divided by resistors R0717 to R0719 with the voltage limit setting VLTG LIMIT SET from the D/A converter (U0731-13) and keeps the control voltage constant via Q0711 if the control voltage, reduced by the resistive divider (R0717 to R0719), approaches the voltage of VLTG LIMIT SET (U0731-13).

Rise and fall time of the output power during transmitter keying and dekeying is controlled by the comparator formed by opamp U0701-3.

During normal transmitter operation the voltage at U701-3 pin 13 is higher than the voltage at pin 12 causing the output at pin 14 being low and switching off transistor Q0711. Diode D0732 reduces the bias voltages BIAS VLTG, BIAS VLTG 2 for low control voltage levels.

The temperature of the PA area is monitored by opamp U0701-1 using thermistor R8641 (located in the PA section). If the temperature increases, the resistance of the thermistor decreases, decreasing the voltage PA TEMP. The inverting amplifier formed by U0701-1 amplifies the PA TEMP voltage and if the voltage at opamp pin 1 approaches 4.6 V plus the voltage (ON) across D0721, U701-1 simulates an increased power which in turn decreases the power control voltage until the voltage at U0701-4 pin 9 is 4.6V again. During normal transmitter operation the output voltage of opamp U701-1 pin 1 is below 4.6V. Diode D8601 located in the PA section acts as protection against transients and wrong polarity of the supply voltage.

10.0 Frequency Synthesis

The complete synthesizer subsystem consists of the Reference Oscillator (U8702), the Fractional-N synthesizer (U8701), the Voltage Controlled Oscillator (Q8802), the RX and TX buffer stages (Q8831, Q8851, Q8852, Q8881) and the feedback amplifier (Q8841).

10.1 Reference Oscillator

The Reference Oscillator (Y8702) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. An analog to digital (A/D) converter internal to U8701 (FRAC-N) and controlled by the microprocessor via serial interface (SRL) sets the voltage at the warp output of U8701 pin 16 to set the frequency of the oscillator. The output of the oscillator (pin 2 of Y8702) is applied to pin 14 (XTAL1) of U8701 via a RC series combination.

10.2 Fractional-N Synthesizer (U8701)

The FRAC-N synthesizer IC (U8701) consists of a pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balance attenuator to balance the high frequency analog modulation and low frequency digital modulation, a 13V positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 9.3 volts.

A voltage of 9.3V applied to the super filter input (U8701 pin 22) supplies an output voltage of 8.6 VDC at pin 18. It supplies the VCO (Q8802), VCO modulation bias circuit (via R8714) and the synthesizer charge pump resistor network (R8723, R8724, R8726). The synthesizer supply voltage is provided by the 5V regulator U8891.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U8701-32), a voltage of 13 VDC is being generated by the positive voltage multiplier circuitry

(D8701-1-3, C8716, C8717). This voltage multiplier is basically a diode capacitor network driven by two (1.05MHz) 180 degrees out of phase signals (U8701-9 and -10).

Output LOCK (U8701-2) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. IC U8701 divides the 16.8 MHz reference frequency down to 2.1 MHz and provides it at pin 11. This signal is used as clock signal by the controller.

The serial interface (SRL) is connected to the microprocessor via the data line SPI DATA (U8701-5), clock line SPI CLK (U8701-6), and chip enable line FRACN CE (U8701-7).

10.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) is formed by the colpitts oscillator FET Q8802. Q8802 draws a drain current of 10 mA from the FRAC-N IC super filter output. The oscillator frequency is half of the desired frequency and mainly determined by L8804, C8809, C8810, C8812 - C8815 and varactor diodes D8802 / D8803. Diode D8804 controls the amplitude of the oscillator.

A balanced frequency doubler T8821, D8821 converts the oscillator fundamental to the desired frequency. With a steering voltage from 2.5V to 10.5V at the varactor diodes the full RX and TX frequency range from 254.9 MHz to 350 MHz is covered.

The doubler output is buffered by common VCO Buffer Q8831 which draws a collector current of 15 mA from the stabilized 5V (U8891). A bandpass filter composed of L8831, C8832 - C8836, 15 nH micro-stripline rejects unwanted harmonics at the first and third oscillator fundamental frequency and matches the output to the following buffer stages. Buffer Q8831 drives the Pre-scaler Buffer Q8841, the PA Buffers Q8851, Q8852 (Pout = 13dBm) and Mixer Buffer Q8881 (Pout = 10dBm). Q8841 draws a collector current of 14 mA from the stabilized 5V, Q8851 draws 15mA, Q8852 draws 20 mA and Q8881 draws 18 mA form the FLT 9V3 source. The buffer stages Q8851, Q8881 and the feedback amplifier Q8841 provide the necessary gain and isolation for the synthesizer loop.

Q8801 is controlled by output AUX3 of U8701 (pin 1) and enables the RX or TX buffer. In RX mode AUX3 is nearly at ground level, in TX mode about 5V DC. In TX mode, with R8802 pulled to ground level by Q8801, the modulation signal coming from the FRAC-N synthesizer IC (U8701 pin28) modulates the VCO via varactor diode D8801 while in RX mode the modulation circuit is disabled by pulling R8802 to a higher level through R8882.

10.4 Synthesizer Operation

The complete synthesizer subsystem works as follows. The output signal of the VCO (Q8802) is frequency doubled by doubler D8821 and, buffered by common VCO Buffer Q8831. To close the synthesizer loop, the collector of Q8841 is connected to the PREIN port of synthesizer U8701 (pin 20). The buffer output (Q8831) also provides signals for the Mixer Buffer Q8881 and the PA Buffers (Q8851, Q8852).

The pre-scaler in the synthesizer (U8701) is basically a dual modulus pre-scaler with selectable divider ratios. This divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SRL. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider´s output signal with the reference signal.The reference signal is generated by dividing down the signal of the reference oscillator (Y8702).

The output signal of the phase detector is a pulsed DC signal which is routed to the charge pump. The charge pump outputs a current at pin 29 (I OUT of U8701). The loop filter (which consists of R8715-R8717, C8723-C8725, C8727) transforms this current into a voltage that is applied to the varactor diodes D8802, D8803 and alters the output frequency of the VCO. The current can be set to a value fixed in the FRAC-N IC or to a value determined by the currents flowing into CPBIAS 1 (U8701-27) or CPBIAS 2 (U8701-26). The currents are set by the value of R8724 or R8726 respectively. The selection of the three different bias sources is done by software programming.

To reduce synthesizer lock time when new frequency data has been loaded into the synthesizer the magnitude of the loop current is increased by enabling the IADAPT line (U8701-31) for a certain software programmable time (Adapt Mode). The adapt mode timer is started by a low to high transient of the FRACN CE line. When the synthesizer is within the lock range the current is determined only by the resistors connected to CPBIAS 1, CPBIAS 2, or the internal current source.

A settled synthesizer loop is indicated by a high level of signal LOCK DET (U8701-2). This signal is routed to uP U0101-17 for further processing.

In order to modulate the PLL the two spot modulation method is utilized. Via pin 8 (MODIN) on U8701 the audio signal is applied to both the A/D converter (low freq path) as well as the balance attenuator (high freq path). The A/D converter converts the low frequency analog modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO's deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U8701-28) and connected to the VCO modulation diode D8801.

Chapter 6.4

300-345MHz Diagrams and Parts Lists

Table of Contents

Description Page

300-345MHz Diagrams and Parts Lists

PCB Layout Component Side 1
PCB Layout Solder Side 2
128ch Model, Controller Schematic Diagram *1 of 2* 3
128ch Model, Controller_IO Schematic Diagram *2 of 2* 5
Parts List 4/6
4ch Model, Controller Schematic Diagram *1 of 2* 7
4ch Model, Controller_IO Schematic Diagram *2 of 2* 9
Parts List 8/10
Supply Voltage Schematic Diagram. 11
Parts List 12
Power Control Schematic Diagram 13
Parts List 14
Power Amplifier 5-25W Schematic Diagram 15
Parts List 16
Synthesizer Schematic Diagram 17
Parts List 18
Voltage Controlled Oscillator Schematic Diagram 19
Parts List 20
RX-FE Schematic Diagram 21
Parts List 22
RX-IF Schematic Diagram 23
Parts List 24

MOTOROLA

GM350

Mobile Radio

Service Manual

66-88MHz Specific Information

CHAPTER 7



Chapter 7

66-88MHz Specific Information

Table of Contents

Chapter

7.1 Model Chart and Test Specifications

7.2 Radio Tuning Procedure

7.3 Theory of Operation

7.4 PCB/Schematic Diagrams and Parts Lists

Chapter 7.1

Model Chart and Test Specifications

Table of Contents

Paragraph		Page
1.0	**Overview**	1
2.0	**Model Chart**	1
3.0	**Test Specifications**	2
3.1	General	2
3.2	Transmitter	2
3.3	Receiver	3
3.4	Self-quieting Frequencies	3

1.0 Overview

This chapter lists the Midband (66-88MHz) models and technical specifications available for the GM350 mobile radio.

2.0 Model Chart

Model	Description
M08FHE4AA2_N	GM350 66-88MHz 12.5 kHz 25W
M08FHF4AA3_N	GM350 66-88MHz 12.5 kHz 25W D
M08FHE6AA2_N	GM350 66-88MHz 20/25 kHz 25W
M08FHF6AA3_N	GM350 66-88MHz 20/25 kHz 25W D

GM350
66-88 MHz Midband

X = Indicates one of each required

					Item	Description
	X	X	X	X	GBN6147_	Packaging Kit
	X		X		GCN6103_	Control Head Model A2 Non-Display
		X		X	GCN6105_	Control Head Model A3 Display
	X	X	X	X	GLN7324_	Low Profile Trunnion Kit
	X	X	X	X	GMN6146_	Enhanced Compact Microphone
		X			GUC1202_	RF & HSG 128ch MB 12.5kHz 5-25W
				X	GUC1203_	RF & HSG 128ch MB 20/25kHz 5-25W
	X				GUC1204_	RF & HSG 4ch MB 12.5kHz 5-25W
			X		GUC1205_	RF & HSG 4ch MB 20/25kHz 5-25W
	X	X	X	X	GKN6270_	Power Cable
	X	X	X	X	68P02923X01	GM350 User Guide M/L
Service Options						
	X				ENUC1003_S	GM350 MB 12.5kHz A2 MD234BA
			X		ENUC1004_S	GM350 MB 25kHz A2 MD214BA
		X			ENUC1005_S	GM350 MB 12.5kHz A3 MD234BB
				X	ENUC1006_S	GM350 MB 25kHz A3 MD214BB

3.0 Technical Specification

3.1 General

SPECIFICATION ITEM	TYPICAL VALUE
Frequency Range	Midband: 66-88 MHz
Channel Spacing	12.5 or 20/25 kHz
Frequency Stability	±5ppm
Power Supply	10.8 to 15.6V dc, negative earth
Dimensions	44x168x160 mm (HxWxD)
Weight	1030g
Operational Temperature	- 25°C to + 55°C
Storage Temperature	- 40°C to + 85°C
Antenna Connection	50Ω BNC
Environmental - Mechanical - Electrical	 Vibration IEC 68/2/27 and Shock IEC 28/2/6 European Dust & Water protection IP54 ETS300-086 RF Specifications ETS300-113 Cyclic Keying Requirements ETS300-279 EMC Requirements ETS300-219 Signalling

3.2 Transmitter

SPECIFICATION ITEM	TYPICAL VALUE
Channel Spacing	12.5 or 20/25 kHz
Output Power	5-25W
Modulation Limiting	<±2.5kHz (12.5kHz); <±4kHz (20kHz); <±5kHz (25kHz)
FM hum & noise (CCITT)	>40dB (12.5kHz); >45dB (25kHz) CCITT
Conducted/Radiated Emission	<0.25uW (0.1...1000MHz); <1uW (1...4GHz)
Adjacent Channel Power	<-60dB (12.5kHz); <-70dB (25kHz)
Audio Response (300 - 3000 Hz)	Flat or pre-emphasised
Audio Distortion	<5% @ 1kHz, 60% deviation
Transmit turn on time	<25msec

3.3 Receiver

SPECIFICATION ITEM	TYPICAL VALUE
Channel Spacing	12.5 or 20/25 kHz
Sensitivity @ 12.5 kHz	< 0.35uV (12dB SINAD)
Sensitivity @ 25 kHz	< 0.35uV (12dB SINAD)
Intermodulation	>65dB ETS; >70dB with Base Option
Adjacent Channel Selectivity	>60dB (12.5kHz); >70dB (20/25kHz) ETS
Spurious Rejection	>70dB ETS
Audio Distortion @ Rated Audio	<5%
Hum and Noise (CCITT)	>40dB (12.5kHz); >45dB (20/25kHz) CCITT
Audio Response (300 - 3000 Hz)	Flat or De-Emphasised
Co-channel Rejection	<12dB (12.5kHz) , <8dB (20/25kHz) ETS
Conducted /Radiated Emission	<2nW (0,1..1000MHz); <20nW (1..4GHz)
Receive after transmit time	<25msec
Audio Output Power	4W (internal speaker); <13W external

3.4 Self-Quieting Frequencies

Self-quieting frequencies are frequencies that are also generated by the radio and cause internal interference. On these frequencies the interference caused by the self-quieter spur is great enough that a radio will not meet its receiver sensitivity specification.

The frequencies are: Midband 67.2, 83.78 and 84MHz.

Chapter 7.2

Radio Tuning Procedure

Table of Contents

Paragraph		Page
1.0	**Midband (66-88MHz) Tuning Procedure**	1
1.1	General	1
1.2	PA Bias Voltage	3
1.3	Battery Threshold	3
1.4	Transmitter Power	4
1.5	Reference Oscillator	4
1.6	Front-End Filter	5
1.7	Rated Volume	6
1.8	Squelch	6
1.9	Transmit Deviation Limit	7
1.10	Transmit Modulation Balance (Compensation)	7

1.0 Midband (66-88MHz) Tuning Procedure

1.1 General

The recommended hardware platform is a 386 or 486 DX 33 PC (personal computer) with 8 MBytes RAM, MS-DOS™ 5.0, Windows™3.1, and RSS (Radio Service Software). These are required to align the radio. Refer to your RSS Installation Manual for installation and setup procedures for the required software; the user manual is accessed (and can be printed if required) via the RSS.

To perform the alignment procedures, the radio must be connected to the PC, RIB (Radio Interface Box), and Universal Test Set as shown in figure 7.2-1.

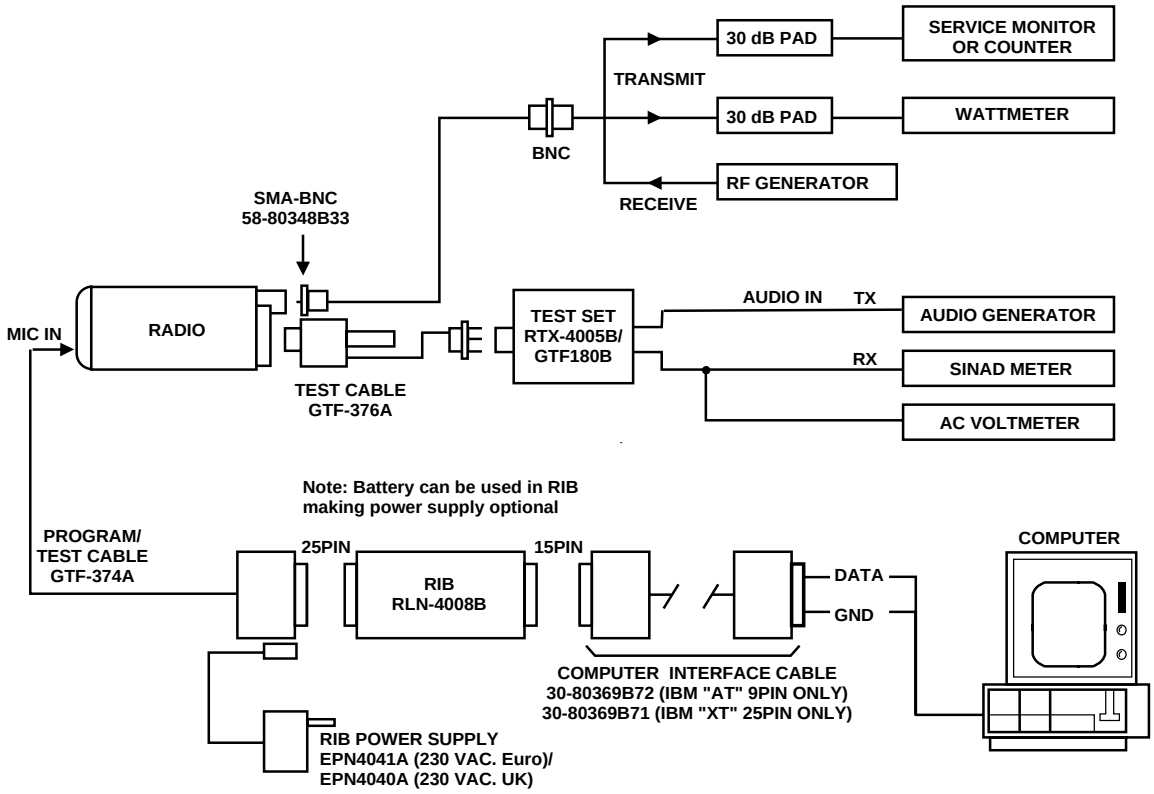


Figure 7.2-1 Radio Alignment Test Setup.

All tuning procedures are performed from the Service menu.

Before going into the Service menu, the radio must first be read using the File / Read Radio menu (if the radio has just been programmed with data loaded from disk or from a newly created codeplug, then it must still be read so that the RSS will have the radio's actual tuning values).

All Service windows read and program the radio codeplug directly; you do NOT have to use the RSS Read Radio / Write Radio functions to program new tuning values.

CAUTION:  **DO NOT** switch radios in the middle of any Service procedure. Always use the Program or Cancel key to close the tuning window before disconnecting the radio. Improper exits from the Service window may leave the radio in an improperly configured state and result in seriously degraded radio or system performance.

The Service windows introduce the concept of the “Softpot”, an analog SOFTware controlled POTentiometer used for adjusting all transceiver alignment controls. A softpot can be selected by clicking with the mouse at the value or the slider or by hitting the TAB key until the value or the slider is highlighted.

Each Service window provides the capability to increase or decrease the ‘softpot’ value with the mouse, the arrow keys or by entering a value with the keyboard. The window displays the minimum, maximum, and step value of the softpot. In addition transmitter tuning windows indicate the transmitter frequency and whether the radio is keyed.

Adjusting the softpot value sends information to the radio to increase (or decrease) a DC voltage in the corresponding circuit. For example, increasing the value in the Reference Oscillator tune window instructs the radio microprocessor to increase the voltage across a varactor in the reference oscillator to increase the frequency. Clicking the Program button stores all the softpot values of the current window permanently in the radio.

In ALL cases, the softpot value is just a relative number corresponding to a D/A (Digital-to-Analog) generated voltage in the radio. All standard measurement procedures and test equipment are similar to previous radios.

Refer to the RSS on-line help for information on the tuning software.

Perform the following procedures in the sequence indicated.

Note: All tuning procedures must be performed at a supply voltage of 13.2V unless otherwise stated. The Modulation Analyser to measure the deviation should be set to frequency modulation with de-emphasis switched off and all high pass filters switched off.

1.2 PA Bias Voltage

Adjustment of the PA Bias is critical for proper radio operation. Improper adjustment will result in poor operation and may damage the PA FET device. For this reason, the PA bias must be set before the transmitter is keyed the first time.

Note: For certain radio models there are two bias voltage settings. For these radios both ‘ Bias 1 Voltage ’ and ‘ Bias 2 Voltage ‘ need to be adjusted when aligning the PA Bias. For models that only have one bias voltage setting, the ‘ Bias 2 Voltage ‘ will be shown in grey on the service menu.

1. From the Service menu, select Tx Alignments.
2. Select Bias Voltage to open the bias voltage tuning window. If the control voltage is out of range, an error message will be displayed. In this case the radio hardware has a problem and tuning must be stopped immediately.
3. Click the Toggle Bias button to set the quiescent current temporarily to 0 mA. The status bar will indicate that the bias is switched off.
4. Measure the DC current of the radio. Note the measured value and add the specified quiescent current shown in table 7.2-1. The result is the tuning target.
5. Click the Toggle Bias button to switch on the quiescent current again.
6. Adjust the current per the target calculated in step 4.
7. Click the Program button to store the softpot value.

Table 7.2-1 Quiescent Current Alignment.

RF-Band	Target
Midband	150mA±15%

1.3 Battery Threshold

The radio uses 2 battery threshold levels Tx High and Tx Low to determine the battery condition.

The Program buttons must only be activated when the power supply is set to the indicated voltage. If the RSS detects that the voltage is not within the expected range for the threshold in question then a message will be displayed to warn that the radio may not be set up correctly for the alignment operation.

CAUTION: Inadvertant Use Of The Program Buttons May Result In Radio Failure.

1. From the Service menu, select Tx Alignments.
2. Select Battery Thresholds to open the battery thresholds tuning window.
3. Set the supply voltage to the value indicated for Tx High.
4. Click the Tx High Program button to store the softpot value for Tx High.
5. Set the supply voltage to the value indicated for Tx Low.
6. Click the Tx Low Program button to store the softpot value for Tx Low.
7. Close the window by clicking Cancel.

1.4 Transmitter Power

The radio has two power level settings, a high power level setting, and a low power level setting.

IMPORTANT: To set the transmitter power for customer applications use the Per Radio window under the Edit menu and set the “Power 1” and “Power 2” powers to the desired values. Only if the transmitter components have been changed or the transmitter does not transmit with the power set in the Per Radio window, should the following procedure be performed.

The advanced power setting technology employed in the radio makes use of two reference power level settings along with parameters describing the circuit behaviour. To determine these parameters the RSS requires the power values measured for two different settings.

1. From the Service menu, select Tx Alignments.
2. Select RF Power to open the RF power tuning window. The window will indicate the transmit test frequencies to be used.
3. Select the Point 1 value of the first frequency.
4. Click the Toggle PTT button to key the radio. The status bar will indicate that the radio is transmitting.
5. Measure the transmitter power on your power meter.
6. Enter the measured value in the box Point 1.
7. Select the Point 2 value of the first frequency.
8. Measure the transmitter power on your power meter.
9. Enter the measured value in the box Point 2.
10. Click the Toggle PTT button to dekey the radio.
11. Repeat steps 3 - 10 for all test frequencies shown in the window.
12. Click the Program button to store the softpot values.

1.5 Reference Oscillator

Adjustment of the reference oscillator is critical for proper radio operation. Improper adjustment will not only result in poor operation, but also a misaligned radio that will interfere with other users operating on adjacent channels. For this reason, the reference oscillator should be checked every time the radio is serviced. The frequency counter used for this procedure must have a stability of 0.1ppm (or better).

1. From the Service menu, select Tx Alignments.
2. Select Reference Oscillator to open the reference oscillator tuning window. The tuning window will indicate the target transmit frquency.
3. Click the Toggle PTT button to key the radio. The status bar will indicate that the radio is transmitting.
4. Measure the transmit frequency on your frequency counter.
5. Adjust the reference oscillator softpot in the tuning window to achieve a transmit frequency within the limits shown in table 7.2-2.
6. Click the Toggle PTT button again to dekey the radio and then click the Program button to store the softpot value.

Table 7.2-2 Reference Oscillator Alignment.

RF-Band	Target
All bands	±150 Hz

1.6 Front-End Filter

Alignment of the front-end pre-selector is normally not required on these radios. Only if the radio has poor receiver sensitivity or the pre-selector parts have been replaced the following procedure should be performed. The softpot value sets the control voltage of the pre-selector. Its value needs to be set at 7 frequencies across the frequency range. If the radio supports 20 or 25 kHz channel spacing selection, use the parameters for 25 kHz channel spacing.

1. Set the test box (GTF180) meter selection switch to the “Audio PA” position and connect a SINAD meter to the “METER” port.
2. From the Service menu, select Rx Alignments.
3. Select Front End Filter to open the pre-selector tuning window. The window will indicate the receive test frequencies to be used.
4. Select the first test frequency shown, and set the corresponding value to the start value shown in table 7.2-4.
5. Set the RF test generator to the receive test frequency, and set the RF level to 10µV modulated with a 1kHz tone at the normal test deviation shown in table 7.2-3.
6. Measure the RSSI voltage at accessory connector pin 15 with a dc voltmeter capable of 1mV resolution and at least 1Mohm input impedance.
7. Change the softpot value by the stepsize shown in table 7.2-4 and note the RSSI voltage.The target softpot value is achieved when the measured RSSI voltage change between step 6 and step 7 is lower than the tuning target for the first time. The tuning target, shown in table 7.2-4, is expressed as the percentage of the measured RSSI voltage and must be recalculated for every tuning step. If the measured RSSI voltage decreases before the target value has been achieved, approximation should be stopped and the current softpot value should be used as target value. Set test box (GTF180) audio switch to the “SPKR” position. The 1 kHz tone must be audible at the target value to make sure the radio is receiving.
8. Repeat steps 4 - 7 for all test frequencies shown in the window.
9. Click the Program button to store the softpot values.

Table 7.2-3 Normal Test Deviation.

Channel Spacing	Deviation
12.5 kHz	1.5 kHz
20 kHz	2.4 kHz
25 kHz	3 kHz

Table 7.2-4 Start Value for Front-End Pre-selector Tuning.

RF-Band	Target	Stepsize	Start Value
Midband	0.29%	+4	Minimum

1.7 Rated Volume

The rated volume softpot sets the maximum volume at normal test modulation.

1. Set test box (GTF180) meter selection switch to the “AUDIO PA” position and the speaker load switch to the “MAXAR” position. Connect an AC voltmeter to the test box meter port.
2. From the Service menu, select Rx Alignments.
3. Select Rated Volume to open the rated volume tuning window. The screen will indicate the receive test frequency to be used.
4. Set the RF test generator to the receive test frequency, and set the RF level to 1mVolt modulated with a 1kHz tone at the normal test deviation shown in table 7.2-3. Set test box (GTF180) audio switch to the “SPKR” position. The 1kHz tone must be audible to make sure the radio is receiving.
5. Adjust the value of the softpot to obtain rated audio volume (as close to 3.87 Vrms)
   Note: The voltage at the meter port of the testbox GTF180 is only half the voltage at the speaker.
6. Click the Program to store the softpot value.

1.8 Squelch

The squelch softpots set the signal to noise ratio at which the squelch opens. The squelch value needs to be set at 7 frequencies across the frequency range. If the radio supports 20 or 25 kHz channel spacing selection, the radio stores separate tuning data for 20 kHz and 25 kHz channel spacing. Therefore, both sets of tuning data should be tuned independently.

1. Set the test box (GTF180) meter selection switch to the “Audio PA” position and connect a SINAD meter to the “METER” port.
2. From the Service menu, select Rx Alignments.
3. Select ‘Squelch’ to open the squelch tuning window. This window is used to set the values for 12.5kHz radios and the 25kHz data for 20/25kHz radios. The window will indicate the receive test frequencies to be used.
4. Select the first test frequency shown, and set the corresponding value to 0.
5. Set the RF test generator to the test frequency and modulate the signal generator at the normal test deviation shown in table 7.2-3, with 1kHz tone. Adjust the generator for a 8-10 dB SINAD level (weighted with psophometric filter).
6. Adjust the softpot value until the squelch just closes.
7. Monitor for squelch chatter; if chatter is present, repeat step 6.
8. When no chatter is detected, select the next softpot and repeat steps 4 - 7 for all test frequencies shown in the window.
9. Click the Program button to store the softpot values.
10. If the radio supports 20 or 25kHz channel spacing selection, repeat steps 2-9 for 20kHz channel spacing using the ‘Squelch (20kHz)’ window.

1.9 Transmit Deviation Limit

The transmit deviation limit softpot sets the maximum deviation of the carrier. The deviation limit needs to be set at 7 frequencies across the frequency range. Unlike other radios, the deviation limit for GM350 is set using low frequency (PL) rather than the usual 1 kHz tone. No audio signal must be injected, the radio generates a 82.5 Hz tone while the deviation limit alignment window is open. This tone is used to set the maximum deviation. If the radio supports 20 or 25 kHz channel spacing selection, the radio stores separate tuning data for 20 kHz and 25 kHz channel spacing. Therefore, both sets of tuning data should be tuned independently

1. From the Service menu, select Tx Alignments.
2. Select 'Deviation Limit' to open the deviation limit tuning window. This window is used to set the values for 12.5 kHz radios and the 25 kHz data for 20/25 kHz radios. The window will indicate the transmit test frequencies to be used.
3. Select the first test frequency shown in the window.
4. Click the Toggle PTT button to key the radio. The status bar will indicate that the radio is transmitting.
5. Adjust the transmitter deviation to the value shown in table 7.2-5.
6. Click the Toggle PTT button to dekey the radio.
7. Repeat steps 3 - 6 for the remaining test frequencies.
8. Click the Program button to store the softpot values.
9. If the radio supports 20 or 25 kHz channel spacing selection repeat steps 1 - 8 for 20 kHz channel spacing using the 'Deviation Limit (20 kHz)' window.

Table 7.2-5 Transmitter Deviation Limit Alignment Target.

Channel Spacing	Deviation
12.5 kHz	375 kHz
20 kHz	600 kHz
25 kHz	750 kHz

1.10 Transmit Modulation Balance (Compensation)

Compensation alignment balances the modulation sensitivity of the VCO and reference modulation (synthesizer low frequency port) lines. Compensation algorithm is critical to the operation of signalling schemes that have very low frequency components (e.g. PL) and could result in distorted waveforms if improperly adjusted. The compensation value needs to be set at 7 frequencies across the frequency range and for every channel spacing supported by the radio.

1. From the Service menu, select Tx Alignments.
2. Select Modulation Balance to open the deviation balance tuning window. This window is used to set the values for 12.5 kHz radios and the 25 kHz data for 20/25 kHz radios. The window will indicate the transmit test frequencies to be used.
3. Set the Test Box (GTF180) meter selector switch to the „GEN" position, and inject a 2 kHz (two kilohertz) tone at 800 mVrms (eight-hundred millivolts) into the "Audio In" port.
4. Connect an AC meter to the meter port to ensure the proper input signal level.
5. Select the first test frequency shown in the window.

6. Click the Toggle PTT button to key the radio. The status bar will indicate that the radio is transmitting.
7. Measure the transmitter deviation.
8. Adjust the transmitter deviation to the value shown in table 7.2-6.
9. Click the Toggle PTT button to dekey the radio.
10. Repeat steps 5 - 9 for the remaining test frequencies.
11. Click the Program button to store the softpot values.
12. If the radio supports 20 or 25 kHz channel spacing selection repeat steps 1 - 11 for 20 kHz channel spacing using the 'Modulation Balance (20kHz)' window.

Table 7.2-6 Transmitter Deviation.

Channel Spacing	Deviation
12.5 kHz	2.2-2.3 kHz
20 kHz	3.4-3.6 kHz
25 kHz	4.3-4.6 kHz

Chapter 7.3

Theory of Operation

Table of Contents

Paragraph		Page
1.0	**Overview**	1
2.0	**Closed Controller**	1
2.1	General	1
2.2	Voltage Regulators	1
2.3	Electronic On/Off	2
2.4	Mechanical On/Off	2
2.5	Ignition	3
2.6	Hook	3
2.7	Microprocessor Clock Synthesizer	3
2.8	Serial Peripheral Interface (SPI)	3
2.9	SPEB Serial Interface	4
2.10	General Purpose Input/Output	4
2.11	Normal Microprocessor Operation	5
2.12	Control Head Model A2 or A3	5
	Controller Board Audio and Signalling Circuits	
3.0	**General**	7
3.1	Audio Filter IC (AFIC)	7
3.2	Audio Ground	7
4.0	**Transmit Audio Circuits**	7
4.1	Mic Input Path	7
4.2	External Mic Path	8
4.3	PTT Sensing and TX Audio Processing	8
4.4	Option Board only (128ch only)	9

Paragraph Page

5.0 Transmit Signalling Circuits 10
5.1 Sub-audible Data (PL/DPL) 10
5.2 High Speed Data and DTMF 11

6.0 Receive Audio Circuits 12
6.1 Squelch Detect 12
6.2 Audio Processing and Digital Volume Control 13
6.3 Audio Amplification Speaker (+) Speaker (-) 13
6.4 Handset Audio 14
6.5 Filtered Audio (128ch only) 14
6.6 Option Board Audio (128ch only) 14

7.0 Receive Signalling Circuits 15
7.1 Sub-audible Data Decoder (PL/DPL) 15
7.2 High Speed Data Decoder 15
7.3 Alert Tone Circuits 16

Midband (66-88MHz) Specific Circuit Description

8.0 Receiver Front-End 17
8.1 Front-End Band-Pass Filter & Pre-Amplifier 17
8.2 Mixer and Intermediate Frequency (IF) Section 17
8.3 IF IC (U2201) 18

9.0 Transmitter Power Amplifier (PA) 5-25W 18
9.1 Power Controlled Stage 18
9.2 PA Stages 19
9.3 Directional Coupler 19
9.4 Antenna Switch 19
9.5 Harmonic Filter 20
9.6 Power Control 20

10.0 Frequency Synthesis 21
10.1 Reference Oscillator 21
10.2 Fractional-N Synthesizer (U2701) 22
10.3 Voltage Controlled Oscillator (VCO) 22
10.4 Synthesizer Operation 23

1.0 Overview

This section provides a detailed theory of operation for the radio and its components. The main radio is a single board design, consisting of the transmitter, receiver, and controller circuits.

The main board is designed to accept one additional option board. This may provide functions such as secure voice/or a signalling decoder.

A control head is either mounted directly on the front of the radio or connected via an extension cable. The control head contains a speaker, LED indicators, a microphone connector, buttons and dependant of radio type, a display. These provide the user with interface control over the various features of the radio.

In addition to the power cable and antenna cable, an accessory cable can be attached to a connector on the rear of the radio. The accessory cable provides the necessary connections for items such as external speaker, emergency switch, foot operated PTT, ignition sensing, etc.

2.0 Controller

2.1 General

The radio controller consists of 4 main subsections:

- ❑ Digital Control
- ❑ Audio Processing
- ❑ Power Control
- ❑ Voltage Regulation

The digital control section of the radio board is based upon a closed architecture controller configuration. It consists of a microprocessor, support memory, support logic, signal MUX ICs, the On/Off circuit, and general purpose Input/Output circuitry.

The controller uses the Motorola 68HC11E9 (U0101) for a 4 channel radio and the 68HC11E20 for a 128 channel radio. In this configuration RAM and ROM are contained within the microprocessor itself. The only external memory device in the closed architecture controller is an EEPROM (U0108) (2KByte for 128 channel radio).

Note: From this point on the 68HC11E9 or E20 microprocessor will be referred to as E9/20µP or µP. References to a Control Head will be to radio model A3 (Display radio).

2.2 Voltage Regulators

Voltage regulation for the controller is provided by 3 separate devices; U0631 (LP2951CM) +5V, U0601 (LM2941T) +9.3V, and UNSW 5V (a combination of R0621 and VR0621). An additional regulator is located in the RF section.

Voltage regulation providing 5V for the digital circuitry is done by U0631. Input and output capacitors (C0631/C0632 and C0633-C0635) are used to reduce high frequency noise and provide proper operation during battery transients. This regulator provides a reset output (pin 5) that goes to 0 volts if the regulator output goes out of regulation. This is used to reset the controller to prevent improper operation. Diode D0631 prevents discharge of C0632 by negative spikes on the 9V3 voltage.

Regulator U0601 is used to generate the 9.3 volts required by some audio circuits, the RF circuitry and power control circuitry. Input and output capacitors (C0601-C0603 and C0604/C0605) are used to reduce high frequency noise. R0602/R0603 set the output voltage of the regulator. If the voltage at pin 1 is greater than 1.3 volts the regulator output decreases and if the voltage is less than 1.3 volts the regulator output increases. This regulator output is electronically enabled by a 0 volt signal on pin 2. Q0601 and associated circuitry (R0601/R0604/R0605) are used to disable the regulator when the radio is turned off.

UNSW 5V is only used in a few areas which draw low current and requires 5 V while the radio is off.

UNSW 5V CL is used to buffer the internal RAM. C0622 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Diode D0621 prevents radio circuitry from discharging this capacitor.

The voltage 9V3 SUPP is only used in the VHF radio (T1) to supply the drain current for the RF MOS FET in the PA.

The voltage SW B+ is monitored by the µP through the voltage divider R0641/R0642 and line BATTERY VOLTAGE. Diode VR0641 limits the divided voltage to 5.1V to protect the µP.

Diode D2601 (MB) located on the PA section acts as protection against transients and wrong polarity of the supply voltage.

2.3 Electronic On/Off

The radio has circuitry which allows radio software and/or external triggers to turn the radio on or off without direct user action. For example, automatic turn on when ignition is sensed and off when ignition is off.

Q0611 is used to provide SW B+ to the various radio circuits. Q0611 acts as an electronic on/off switch controlled by Q0612. The switch is on when the collector of Q0612 is low. When the radio is off Q0612 is cutoff and the voltage at Q0611-base is at A+. This effectively prevents current flow through Q0611 from emitter to collector. When the radio is turned on the voltage at the base of Q0612 is high (about 0.6V) and Q0612 switches on (saturation) and pulls down the voltage at Q0611-base. With Transistor Q0611 now enabled current flows through the device. This path has a very low impedance (less than 1 ohm) from emitter to collector. This effectively provides the same voltage level at SWB+ as at A+.

The electronic on/off circuitry can be enabled by the microprocessor (through AFIC port GCB1, line B+ CONTROL), the mechanical On/Off button on the control head (line ON OFF CONTROL), or the ignition sense circuitry (line IGNITION CONTROL). If any of the 3 paths cause a low at the collector of Q0612, the electronic ON is engaged.

2.4 Mechanical On/Off

This refers to the on/off button, located on the control head, and which turns the radio on and off. If the radio is turned off and the on/off button is pressed, line ON OFF CONTROL goes high and switches the radio on as long as the button is pressed. The microprocessor is alerted through line ANALOG 3 which is pulled to low by Q0925 (Control Head with display - A3) while the on/off button is pressed. If the software detects a low state it asserts B+ CONTROL via AFIC pin 39 high which keeps Q0612 and Q0611, and in turn the radio switched on.

If the on/off button is pressed and held while the radio is on, the software detects the line ANALOG 3 changing to low and switches the radio off by setting B+ CONTROL to low.

2.5 Ignition

Ignition sense is used to prevent the radio from draining the vehicle's battery because the engine is not running.

When the IGNITION input (J0400-10) goes above 6 volts Q0612 is turned on via line IGNITION CONTROL. Q0612 turns on SW B+ by turning on Q0611 and the microprocessor starts execution. A high IGNITION input reduces the voltage of line IGNITION SENSE by turning on Q0421. The software reads the line IGNITION SENSE, determines from the level that the IGNITION input is active and sets the B+ CONTROL output of the AFIC pin 39 to high to latch on SW B+.

When the IGNITION input goes below 6 volts, Q0421 switches off and R0426, R0427 pull line IGNITION SENSE high. The software is alerted by line IGNITION SENSE to switch off the radio by setting B+ CONTROL to low. The next time the IGNITION input goes above 6 volts the above process will be repeated.

2.6 Hook

The HOOK input is used to inform the µP when the Microphone´s hang-up switch is engaged. Dependent on the radio model the µP may take actions like turning the audio PA on or off. The signal is routed from J0101-3 and J0400-14 through transistor Q0137 to the µP U0101-56. The voltage range of HOOK in normal operating mode is 0-5V. If a rear GP input line is set as HOOK then the front HOOK signal is overriden

2.7 Microprocessor Clock Synthesizer

The controller uses the oscillator in the microprocessor (U0101) along with some external components (C0115-C0117, L0114, R0115, Y0114) to generate the clock. Q0114 is used to alter the clock frequency slightly under software control if there is a possibility of harmonics of this clock source interfering with the desired radio receive frequency.

2.8 Serial Peripheral Interface (SPI)

The µP communicates to many of the IC's through its SPI port. This port consists of SPI TRANSMIT DATA (MOSI) (U0101-52), SPI RECEIVE DATA (MISO) (U0101-51), SPI CLK (U0101-53) and chip select lines going to the various IC's, connected on the SPI PORT (BUS). This BUS is a synchronous bus, in that the timing clock signal CLK is sent while SPI data (SPI TRANSMIT DATA or SPI RECEIVE DATA) is sent. Therefore, whenever there is activity on either SPI TRANSMIT DATA or SPI RECEIVE DATA there should be a uniform signal on CLK. The SPI TRANSMIT DATA is used to send serial from a µP to a device, and SPI RECEIVE DATA is used to send data from a device to a µP. The only device from which data can be received via SPI RECEIVE DATA is the EEPROM (U0108)

On the controller there are three ICs on the SPI BUS, AFIC (U103-33), EEPROM (U0108-1) and D/A (U0731-6). In the RF sections there is one IC on the SPI BUS, the FRAC-N Synthesizer. The SPI TRANSMIT DATA and CLK lines going to the RF section are filtered by L0194/L0195 to minimize noise. The chip select lines for the IC´s are decoded by the address decoder U102.

The SPI BUS is also used for the control head. U0104-1,2 buffer the SPI TRANSMIT DATA and CLK lines to the control head. U0104-3 switches off the CLK signal for the LCD display if it is not selected via LCD CE and Q0138.

When the μP needs to program any of these IC's it brings the chip select line for that IC to a logic 0 and then sends the proper data and clock signals. The amount of data sent to the various IC's are different, for example the FRAC-N can receive up to 13 bytes (97 bits) while the DAC can receive up to 3 bytes (24 bits). After the data has been sent the chip select line is returned to a logic 1.

The Option board interfaces are different in that the μP can also read data back from devices connected. The timing and operation of this interface is specific to the option connected, but generally follows the pattern:

1) an option board device generates a service request via J0102-7, Q0471, R0472 and μP pin 63,
2) main board asserts a chip select for that option board device via U0102-10, J0102-5,
3) the main board μP generates the CLK (J0102-6), and
4) the main board μP writes serial data via J0102-4 and reads serial data via J0102-2 and, when data transfer is complete the main board terminates the chip select and CLK activity.

2.9 SPEB Serial Interface

The SBEP serial interface allows the radio to communicate with the Radio Service Software (RSS) via the Radio Interface Box (RIB). This interface connects to the Microphone connector (J0903/ J0803) via Control Head connector (J0101-15) or to the accessory connector J0400-6 and comprises BUS+. The line is bi-directional, meaning that either the radio or the RSS can drive the line.

When the RSS needs to communicate with the radio, an interrupt is generated by the BUS+ signal through R0104 and μP pin 47. The μP then starts serial data communication on BUS+ by sending data from pin 50 through D0101 and receiving data at pin 47 through R0104. While the radio is sending serial data at pin 50 it receives an "echo" of the same data at pin 47.

2.10 General Purpose Input/Output

The Controller provides six general purpose lines (GP1 through GP6) available on the accessory connector J0400 to interface to external options. Lines GP1,4 are inputs, GP2 is an output and GP3,5,6 are bidirectional. The software and the hardware configuration of the radio model define the function of each port. Some ports are not connected on the 4ch radio, refer to appendix B for more details.

GP1 can be used as external PTT input or others, set by the RSS.

GP2 can be used as normal output (Q0441 placed) or external alarm output (Q0442 placed). The voltage range can be set by R0442 (0-5V) or R0443 (0 - supply voltage).

GP4 can be used as normal input (D0471, R0477 not placed) or emergency input (D0471, R0477 placed).

GP3,5,6 are bidirectional and use the same circuit configuration. Each port uses an output transistor controlled by μP port PB5,4,7 and an input transistor read by μP port PC2,5,3. To use one of the GP´s as input the μP must turn off the corresponding output transistor.

In addition the signals from GP3-6 are fed to the option board connectors J0102, J0103.
The 470pF and 10nF capacitors serve to filter out any AC noise which may ride on the GP lines.

2.11 Normal Microprocessor Operation

The E9/20µP (U0101) contains internal 12 (E9) or 20 (E20) Kilobytes ROM, 512 (E9) or 768 (E20) bytes SRAM and 512 bytes EEPROM.

The E9/20µP RAM is always powered to maintain parameters such as the last operating mode. This is achieved by maintaining 5V at U0101-25. Under normal conditions, when the radio is off UNSW +5V is formed by FLT A+ running to D0621.

C0622 allows the battery voltage to be disconnected for a couple of seconds without losing RAM parameters. Diode D0621 prevents radio circuitry from discharging this capacitor.

U0101-22 is the high reference voltage for the A/D ports on the E9/20µP. Resistor R0105 and capacitor C0105 filter the +5V reference. If this voltage is lower than +5V the A/D readings will be incorrect. Likewise U0101-21 is the low reference for the A/D ports. This line is normally tied to ground. If this line is not connected to ground, the A/D readings will be incorrect.

The MODB (U0101-25) input of the E9/20µP must be at a logic 1 for it to start executing correctly. The XIRQ (U0101-45) and the IRQ (U0101-46) pins should also be at a logic 1.

Optional external EEPROM (U0108) is available on 128ch radio models. The external EEPROM is accessed through a serial connection. The E9/20µP generates SPI CLK (U0101-53), SPI TRANSMIT DATA (MOSI) (U0101-52) and SPI RECEIVE DATA (MISO) (U0101-51) to read or write EEPROM. On a read of EEPROM the E9/20µP continues generating the clock and the EEPROM places the requested data on the SPI RECEIVE DATA (MISO) line. On a write the message is followed by the data to be written to the EEPROM.

2.12 Control Head Model A2 or A3

The Control Heads contains the internal speaker, the microphone connector, several buttons to operate the radio, and several indicator Light Emitting Diodes (LED) to inform the user about the radio status.

Additionally for A3 model, the control head uses a 3 digit / 7 segment Liquid Crystal Display (LCD) for the numerical information e.g. channel number, select code.

2.12.1 Power Supplies

The power supply to the Control Head is taken from the host radio's FLT A+ voltage via connector J0801(A2) / J0901(A3) pin 8 and the regulated +5V via connector J0801(A2) / J0901(A3) pin 3. The voltage FLT A+ is at battery level and is used for the LEDs, the back light and to power up the radio via the On / Off button. The stabilized +5 volt is used for the (display, the display driver,-A3 only) the shiftregister and the keypad buttons.

2.12.2 Power On / Off

The On/Off button when pressed switches the radio's voltage regulators on by pulling ON OFF CONTROL to high via D0825(A2) / D0925(A3) and connects the base of D0825(A2) / D0925(A3) to FLT A+. This transistor pulls the line ANALOG 3 to low to inform the µP that the On/Off button is pressed. If the radio is switched off, the µP will switch it on and vice versa. If the On/Off button is pressed and held while the radio is on, the software detects a low state on line ANALOG 3 and switches the radio off.

2.12.3 Keypad Keys

The Control Head keypad has 9(A2) / 11(A3) - keys. All keys are configured as 3 analogue lines (ANALOG 1 2 3) to the radio. Lines ANALOG 1,2 each control four keys; line ANALOG 3 controls one(A2) / three (A3) key(s). The voltage on the analogue lines varies between 0V and +5V depending on which key has been pressed. If a button is pressed, it will connect one of the 3 lines ANALOG 1,2,3 to a resistive voltage divider connected to +5V. The voltages of the lines are A/D converted inside the µP and specify the pressed button.

2.12.4 Status LED and Back Light Circuit

All the indicator LEDs 8(A2) / 4(A3) and the back light LEDs 8(A2) / 20(A3) are driven by current sources Q0942 - Q0948, Q0961, Q0962(A2) / Q0942 - Q0944, Q0951, Q0952(A3) and controlled by the µP via SERIAL PERIPHERAL INTERFACE (SPI). The current is determined by the resistor at the emitter of the respective current source transistor. Shiftregister U0841(A2) / U0941(A3) stores the LED status. To update the LED status line LED CLCK BUF shifts the data of line SPI DATA BUF into the shiftregister. When all the data has been written, line LED CE is set to low for a few microseconds to update the output of the shiftregister with the new data.

2.12.5 Liquid Crystal Display (LCD) (A3 model only)

The LCD display H0931 is a 3 digit / 7 segment display which incorporates 9 annunciators. Data is loaded serially into the display driver U0932 via the SPI interface. The display data of line SPI DATA BUF is shifted serially into the display driver by clock signal LCD CLCK BUF. When the last bit has been received, the LCD display is updated.

2.12.6 Microphone Connector

Signals BUS+, PTT, HOOK VPP, MIC HI, HANDSET AUDIO from the microphone connector J0803(A2) / J0903(A3) are fed to the radio's controller section via connector J0801(A2) / J0901(A3).

2.12.7 Speaker

The Control Head contains a speaker for the receiver audio. The receiver audio signal from the differential audio output of the audio amplifier located on the radio's controller is fed via lines INT SPKR+, INT SPKR-, connector J0801-18,17(A2) / J0901-18,17(A3) to the speaker connector J0802(A2) / J0902(A3) pin 1 and pin 2. The speaker is connected to the connector J0802(A2) / J0902(A3).

2.12.8 Electrostatic Transient Protection

Electrostatic transient protection is provided for the sensitive components in the Control Head by diodes VR0801 - VR0809(A2) / VR0901 - VR0909(A3). The diodes limit any transient voltages to tolerable levels. The associated capacitors provide Radio Frequency Interference (RFI) protection.

2.12.9 Reversible Control Head

The control head is connected to the RF transceiver by means of a short flexible ribbon cable. This allows the control head to be mounted either way up in relation to the body of the transceiver. This means that the transceiver can be mounted in the most cosmetically pleasing and most efficient cooling orientation and still have the user interface the "right way" up.

CONTROLLER BOARD AUDIO AND SIGNALLING CIRCUITS

3.0 General

3.1 Audio Filter IC (AFIC)

The AFIC (U0103) used in the controller performs RX/TX audio shaping, i.e. filtering, amplification, attenuation.

The AFIC is programmable through the SPI BUS (U0103-30/31/33), normally receiving 6 bytes. This programming sets up various paths within the AFIC to route audio signals through the appropriate filtering, gain and attenuator blocks. The AFIC also has 4 General Control Bits GCB1,3-5 which are CMOS level outputs. GCB1 is used to switch the radio on and off under µP control via line B+ CONTROL. GCB3 is used to switch the audio PA on and off (AUDIO PA ENABLE). GCB4 selects between the UNATTEN RX OUT audio signal and the unfiltered DET AUDIO signal. GCB5 HIGH LOW BAND can be used to switch between band splits.

3.2 Audio Ground

VAG is the dc bias used as an audio ground for the op-amps that are external to the Audio Filter IC (AFIC). U0105-1 forms this bias by dividing 9.3V with resistors R0171, R0172 and buffering the 4.65V result with a voltage follower. VAG emerges at pin 1 of U0105-1. C0172 is a bypass capacitor for VAG. The AFIC generates its own 2.5 V bias for its internal circuitry. C0153 is the bypass for the AFIC's audio ground dc bias. Note that while there are AFIC VAG, and BOARD VAG (U0105-1) each of these are separate; they do not connect together.

4.0 Transmit Audio Circuits

Refer to Figure 7.3-1 for reference for the following sections.

4.1 Mic Input Path

The radio supports 2 distinct microphone paths known as internal (from Control Head) and external mic (from accessory connector J0400-2) and in 128 channel radios an auxiliary path (FLAT TX AUDIO). The microphones used for the radio require a DC biasing voltage provided by a resistive network.

These two microphone audio inputs are connected together. Following the internal mic path; the microphone is plugged into the radio control head and is connected to the controller board via J0101-16. From here the signal is routed to C0142. R0141 and R0142 provide the 9.3VDC bias. R0142 and C0141 provide a 1kohm AC path to ground that sets the input impedance for the microphone and determines the gain based on the emitter resistor in the microphone's amplifier circuit.

The MIC signal is routed to the AFIC´s TX IN input (U0103-10) through R0146 and R0145 (4 channel radio) or through op-amp buffer U0106-2 and R0145 (128 channel Radio). In radio models which use an option board the signal is routed via option board connector J0103-3,1. The audio signal at the output of U0106-2 should be approximately 80mV for 1.5kHz or 3kHz of deviation with 12.5kHz or 25kHz channel spacing.

In 128 channel radios the FLAT TX AUDIO signal from accessory connector U0400-5 is buffered by op-amp U0106-1 and fed to the AFIC U0103-13 through gate U0107-1. Gate U0107-1 is controlled by the µP port PC7 (U0101-42) and selects between FLAT TX AUDIO or signalling signal created by the µP.

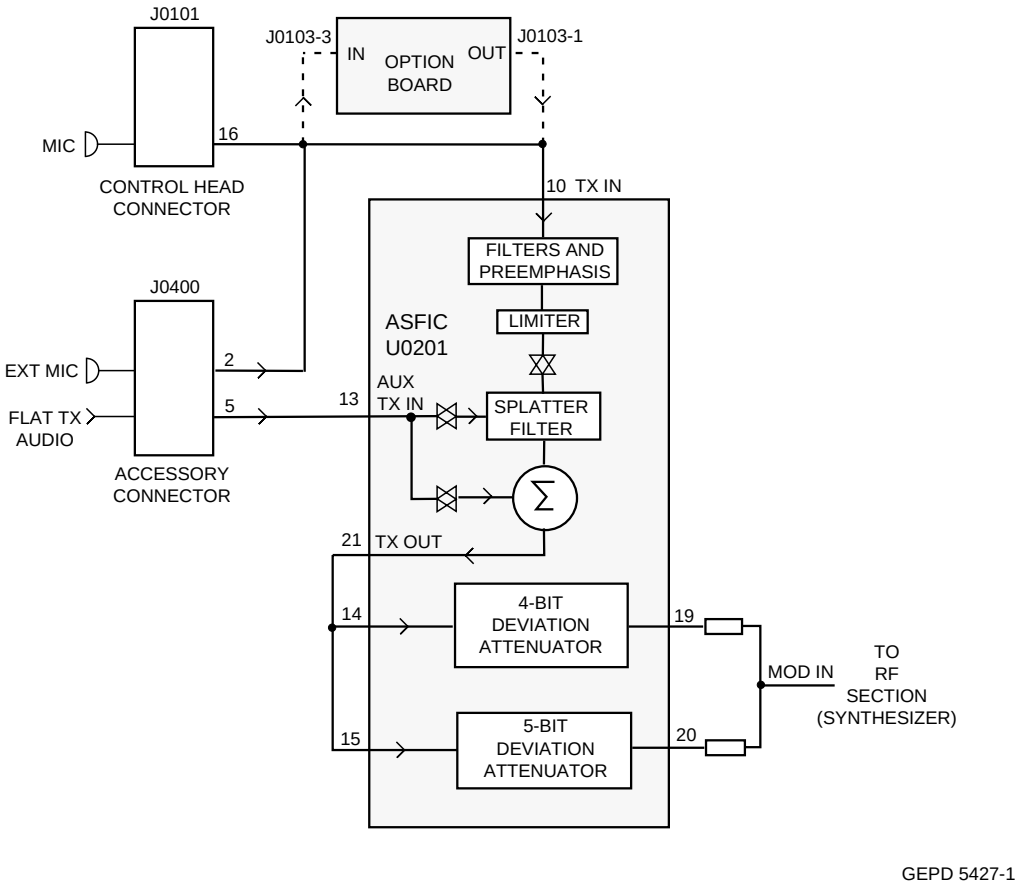


Figure 7.3-1 Transmit Audio Paths

4.2 External Mic Path

The external microphone signal enters the radio on accessory connector J0400 pin 2 and connects to the standard microphone input.

4.3 PTT Sensing and TX Audio Processing

Mic PTT coming from the Control Head via connector J0101-4 is sensed by the uP U0101-39 port PC4 . An external PTT can be generated by grounding pin 3 on the accessory connector if this input is programmed for PTT. The lines MIC and EXTERNAL MIC AUDIO (J0400-2) are connected together.

The MIC signal is routed to the AFIC (U0103) through R0146 and R0145 (4 channel radio) or through op-amp buffer U0106-2 and R0145 (128 channel Radio). In radio models which use an option board the signal is routed via option board connector J0103-3,1. R0145, C0145, the amplifier inside the AFIC (pins 9,10) and gain setting resistors R0147, R0149 pre-emphasise the MIC audio signal.

Inside the AFIC, the MIC audio is filtered to eliminate frequency components outside the 300-3000Hz voice band. The signal is then limited to prevent the transmitter from over deviating. The limited MIC audio is then routed through a summer, which is used to add in signalling data, and then to a splatter filter to eliminate high frequency spectral components that could be generated by the limiter. A summer following the splatter filter adds the signal from the FLAT TX AUDIO input. The capacitor between AFIC TX OUT U0103-21 and AFIC ATTEN IN U0103-14,15 AC couples the signal between AFIC blocks and prevents the DC bias at the AFIC output U0103-19,20 from shifting when the AFIC transmit circuits are powered up. The audio is then routed to two attenuators, which are tuned in the factory or the field to set the proper amount of FM deviation. The TX audio emerges from the AFIC at U0103-19,20. Both signals are weighted by resistors R0181, R0182 and add up to signal MOD IN, at which point it is routed to the RF section.

4.4 Option Board Audio (128 channel model A3 only)

The audio coming from the microphone (J0101-16) or the external microphone (J0400-2) is routed through op-amp buffer U0106-2 (128ch only) to the option board connector J0103-3. After option board processing the signal emerges at J0103-1. The source resistor of the option board output and C0145, the amplifier inside the AFIC (U0103-9,10) and gain setting resistor R0147, R0149 pre-emphasise the signal. Inside the AFIC the signal follows a path identical to conventional transmit audio. The modulation signal emerges from the AFIC at J0103-19/20. Both signals are weighted by resistors R0181, R0182 and add up to signal MOD IN.

5.0 Transmit Signalling Circuits

Refer to Figure 7.3-2 for reference for the following sections. From a hardware point of view, there are three types of signalling:

1. Sub-audible data (PL/DPL/Connect Tone) which is summed with transmit voice or signalling,
2. DTMF data for telephone communication in trunked and conventional systems, and
3. Audible signalling including Select 5, MPT-1327, MDC, High speed Trunking.

All three types are supported by the hardware while the radio software determines which signalling type is available. Currently only PL/DPL and Single tones are supported in the software.

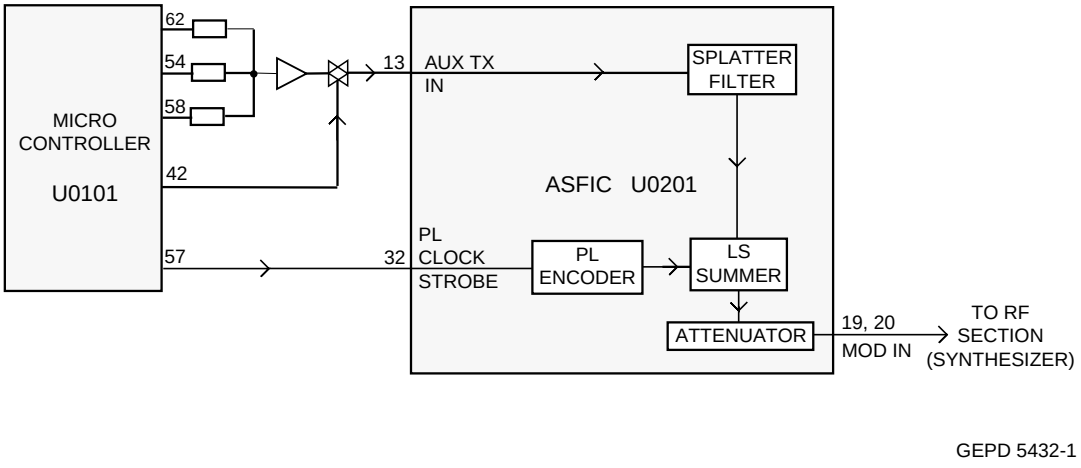


Figure 7.3-2 Transmit Signalling Paths

5.1 Sub-audible Data (PL/DPL)

Sub-audible data implies signalling whose frequency is below 300Hz. Although it is referred to as ”sub-audible data,” the actual frequency spectrum of these waveforms may be as high as 250 Hz, which is audible to the human ear. However, the radio receiver filters out any audio below 300Hz, so these tones are never heard in the actual system.

Only one type of sub-audible data can be generated by U0103 (AFIC) at any one time. The process is as follows, using the SPI BUS, the μP programs the AFIC to set up the proper low-speed data deviation and select the PL or DPL filters. The μP then generates a square wave which strobes the AFIC PL / DPL encode input PL CLOCK STROBE U0103-32 at twelve times the desired data rate. For example, for a PL frequency of 103Hz, the frequency of the square wave would be 1236Hz.

This drives a tone generator inside U0103 which generates a staircase approximation to a PL sine wave or DPL data pattern. This internal waveform is then low-pass filtered and summed with voice or data. The resulting summed waveform then appears on U0103-19,20 (MOD IN), where it is sent to the RF board as previously described for transmit audio.

5.2 High Speed Data and DTMF

The High Speed Data and DTMF waveforms are created by the µP U0101 using summer U0105-3. Op-amp U0105-3 and resistors R0121-R0124 add up the three signals coming from the µP pins 58, 59 and 62. The output signal of U0105-3 is routed to the AFIC (U0103-13) through gate U0107-1 (128ch) or R0130 (4ch). Inside the AFIC the signal enters the conventional transmitter audio path at the splatter filter input. Gate U0107-1 (128ch) controlled by µP port PC7 (U0101-42) selects between data signal and FLAT TX AUDIO signal. Microphone audio is muted during High Speed Data signalling.

6.0 Receive Audio Circuits

Refer to Figure 7.3-3 for reference for the following sections.

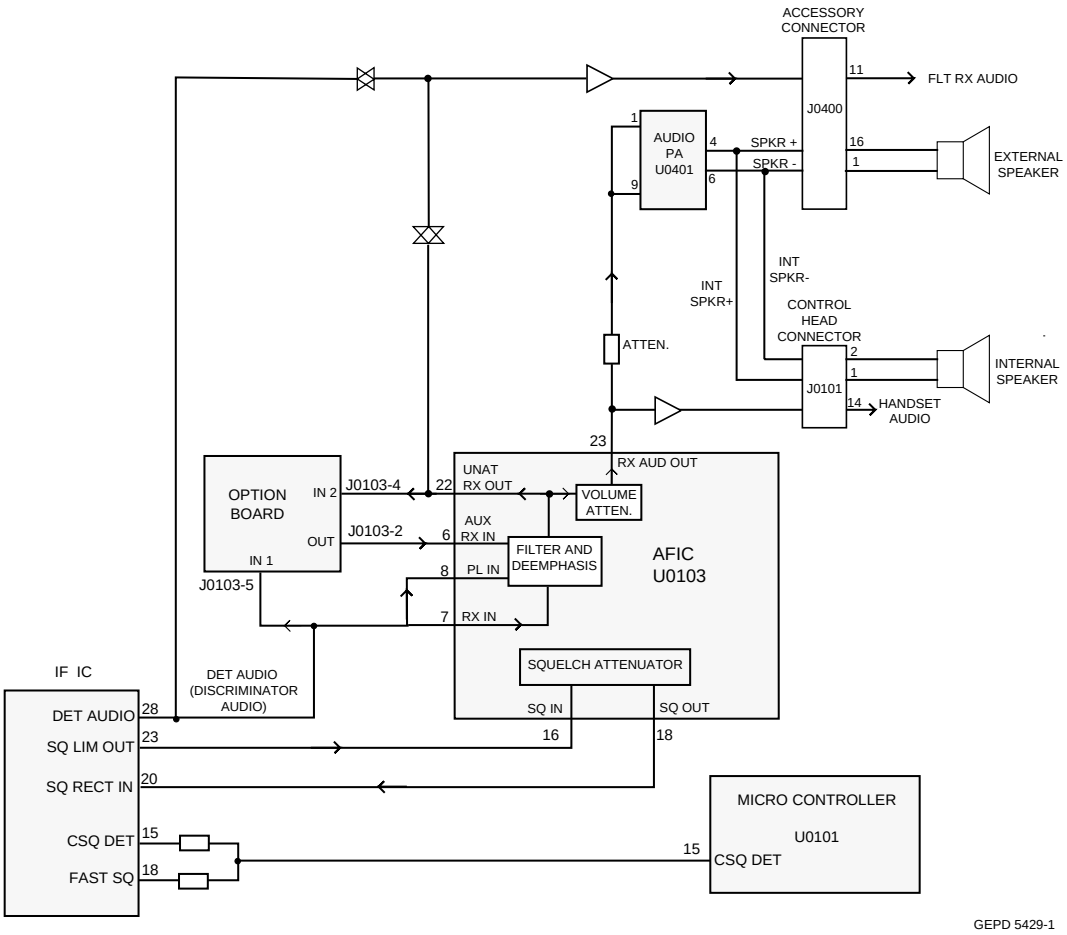


Figure 7.3-3 Receive Audio Paths.

6.1 Squelch Detect

The IF IC controls the squelch characteristics of the radio. With a few external parts (R2221, R2222, C2225, C2226, C2229, C2230, R2223) the squelch tail, hysteresis, attack and delay are optimized for the radio. To set the squelch threshold the signal from IF IC pin 23 (line SQ ATT IN) is routed to the squelch attenuator input of the AFIC (U0103-16). The attenuated signal (line SQ ATT OUT) from the AFIC (U0103-18) enters the IF IC at pin 20 and is used to create a squelch indicator signal available at pin 15 (line CSQ DET).

The microprocessor controlled ADAPT signal at pin 22 activates the fast squelch indicator signal at IF IC pin 18 (FAST SQ). Both squelch indicator signals CSQ DET (pin 15) and FAST SQ (pin 18) are combined, weighted by resistors R0111 / R012 and fed to one of the microprocessor´s ADCs (U0101-15) for interpretation. From the voltage weighted by the resistors the µP determines whether CSQ DET, FAST SQ or both are active.

6.2 Audio Processing and Digital Volume Control

The receiver audio signal enters the controller section from the IF IC (U2201-28) on DET AUDIO. The signal is AC coupled by C0181 and C0182 and enters the AFIC via the RX IN pin U0103-7 and PL DPL IN U0103-8.

Inside the AFIC the signal entering RX IN (U0103-7) goes through the audio path while the signal entering PL DPL IN (U0103-8) goes through the PL/DPL path.

The audio path has a programmable amplifier, whose setting is based on the channel bandwidth being received, then a LPF filter to remove any frequency components above 3000Hz and then an HPF to remove any sub-audible data below 300Hz. Next, the recovered audio passes through a de-emphasis filter if it is enabled (to compensate for Pre-emphasis which is used to reduce the effects of FM noise). The IC then passes the audio through the 8-bit programmable attenuator whose level is set depending on the value of the volume control. Finally, the filtered audio signal passes through an output buffer within the AFIC. The audio signal exits the AFIC at RX AUDIO U0103-23.

The μP programs the attenuator, using the SPI BUS, based on the volume setting. The minimum/ maximum settings of the attenuator are set by codeplug parameters.

Since sub-audible signalling is summed with voice information on transmit, it must be separated from the voice information before processing. Any sub-audible signalling enters the AFIC from the IF IC at PL DPL IN U0103-8. Once inside it goes through the PL/DPL path. The signal first passes through one of 2 low pass filters, either PL low pass filter or DPL/LST low pass filter. Either signal is then filtered and goes through a limiter and exits the AFIC at PL DPL DECODER OUT U0103-27. At this point the signal will appear as a square wave version of the sub-audible signal which the radio received. The microprocessor (U0101-64) will decode the signal directly to determine if it is the tone/ code which is currently active on that mode.

6.3 Audio Amplification Speaker (+) Speaker (-)

The output of the AFIC´s digital volume pot, U0103-23 is routed through a voltage divider formed by R0401 and R0402 to set the correct input level to the audio PA (U0401). This is necessary because the gain of the audio PA is 46 dB, and the AFIC output is capable of overdriving the PA unless the maximum volume is limited.

The audio then passes through C0401 which provides AC coupling and low frequency roll-off. C0402 provides high frequency roll-off as the audio signal is routed to pins 1 and 9 of the audio power amplifier U0401.

The audio power amplifier has one inverted and one non-inverted output that produces the differential audio output SPK+ / SPK- (U0401-4/6). The inputs for each of these amplifiers are pins 1 and 9 respectively; these inputs are both tied to the received audio. The audio PA's DC biases are not activated until the audio PA is enabled at pin 8.

The audio PA is enabled via AUDIO PA ENABLE signal from the AFIC (U0103-40). When the base of Q0401 is low, the transistor is off and U0401-8 is high, using pull up resistor R0406, and the Audio PA is ON. The voltage at U0401-8 must be above 8.5VDC to properly enable the device. If the voltage is between 3.3 and 6.4V, the device will be active but has its input (U0401-1/9) off. This is a mute condition which is not employed in this radio design. R0404 ensures that the base of Q0401 is high on power up. Otherwise there may be an audio pop due to R0406 pulling U0401-8 high before the software can switch on Q0401.

The SPK+ and SPK- outputs of the audio PA have a DC bias which varies proportionately with FLT A+ (U0401-7). FLT A+ of 11V yields a DC offset of 5V, and FLT A+ of 17V yields a DC offset of 8.5V. If either of these lines is shorted to ground, it is possible that the audio PA will be damaged. SPK+ and SPK- are routed to the accessory connector (J400-16 and 1) and to the control head (connector J0101-1 and 2).

6.4 Handset Audio

Certain hand held accessories have a speaker within them which require a different voltage level than that provided by U0401. For those devices HANDSET AUDIO is available at J0101-14.

The received audio from the output of the AFIC´s digital volume attenuator is also routed to U0105-4 pin 9 where it is amplified 15 dB; this is set by the 10k/68k combination of R0154 and R0155. This signal is routed from the output of the op amp U0105-4 pin 8 to J0101-14. The control head sends this signal directly out to the microphone jack. The maximum value of this output is 6.6Vp-p.

6.5 Filtered Audio (128 channel model A3 only)

The AFIC has an audio whose output at U0103-22 has been filtered and de-emphasized, but has not gone through the digital volume attenuator. From AFIC U0103-22 the signal is routed through gate U0107-2 and AC coupled to U0106-4. The gate controlled by AFIC port GCB4 (U0103-2) selects between the filtered audio signal from the AFIC or the unfiltered discriminator signal DET AUDIO from the IF IC.The output at U0106-4 is then routed to J0400-11. Note that any volume adjustment of the signal on this path must be done by the accessory.

6.6 Option Board Receive Audio (128 channel model A3 only)

Discriminator audio from the IF IC or filtered audio UNAT RX OUT from the AFIC (U0103-22) enters the option board at connector J0103-5 and J0103-4. On the option board, the signal may be processed, and then fed back through (J0103-2) to AUX RX IN of the AFIC (U0103-6). From then on it follows a path identical to conventional receive audio, where it is filtered (0.3 - 3kHz) and de-emphasized.

7.0 Receive Signalling Circuits

Refer to Figure 7.3-4 for reference for the following sections.

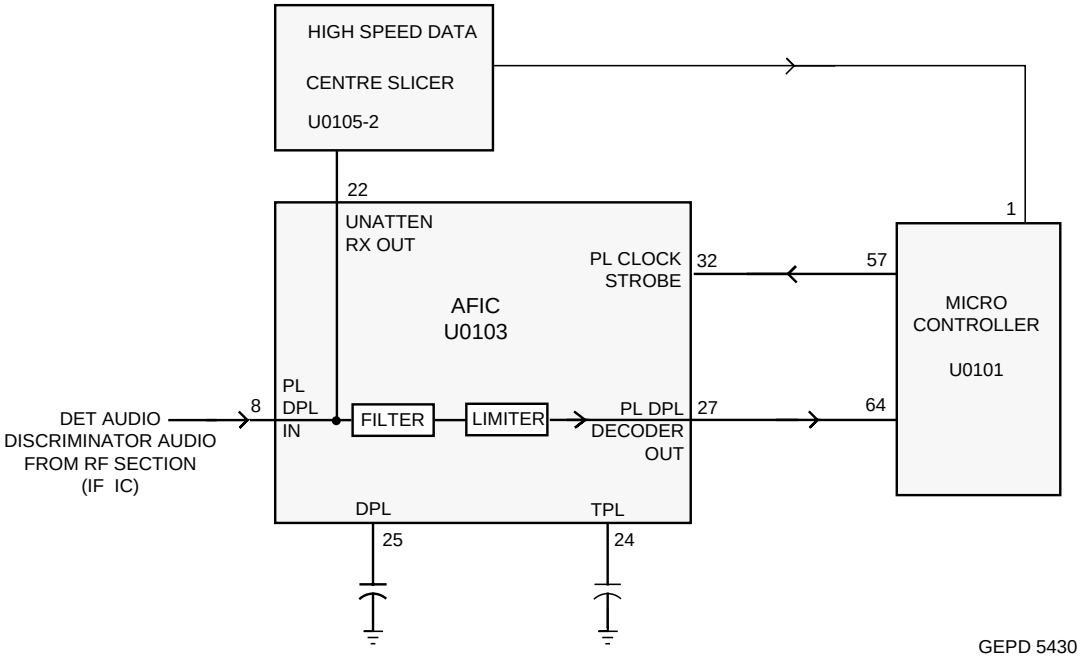


Figure 7.3-4 Receive Signalling Path.

7.1 Sub-audible Data Decoder (PL/DPL)

The receiver audio signal entering the AFIC U0103 at pin 8 first passes through the Tone PL filter or the Digital PL filter, depending on the PL option selected for the current operating mode. Filtered PL is then coupled to the PL detector circuit, with detected PL output at U0103-27. At this point the signal will appear as a square wave version of the sub-audible signal which the radio received. The microprocessor U0101-64 will decode the signal directly to determine if it is the tone / code which is currently active on that mode.

7.2 High Speed Data Decoder

The unattenuated receiver audio signal from U0103-22 is AC coupled to the input of centre slicer circuit U0105-2. The non-inverting input of op-amp U0105-2 is fed through resistor R0162. Capacitor C0164 sets a low-pass corner frequency of 3.3kHz. The inverting input of op-amp U0105-2 is fed through resistor R0163. Capacitor C0163 sets a low-pass corner frequency of 16Hz.

During operation, R0163 / C0163 establish an average DC offset level at U0105-2 pin 6 dependent on the average DC level of the undetected signal to set the “trigger” threshold of U0105-2. R0162 / C0164 provide high audio frequency roll-off to improve falsing immunity, but passes 600 or 1200 baud signals. The detected output from the centre slicer circuit is buffered and inverted by Q0161 and then coupled to the µP U0101-1 where algorithms perform the final decoding.

7.3 Alert Tone Circuits

When the software determines that it needs to give the operator an audible feedback (for a good key press, or for a bad key press), or radio status (trunked system busy, phone call circuit failures), it sends an alert tone to the speaker.

It does so by sending SPI BUS data to U0103 which sets up the audio path to the speaker for alert tones. The alert tone itself is generated by the AFIC.

The allowable internal alert tones are 410, 820, and 1640Hz. In this case a code contained within the SPI BUS load to the AFIC sets up the path and determines the tone frequency, and at what volume level to generate the tone. (It does not have to be related to the voice volume setting).

The output of the generator is summed into the audio chain just after the RX audio de-emphasis block. Inside U0103 the tone is amplified and filtered, then passed through the 8-bit digital volume attenuator, which is typically loaded with a special value for alert tone audio. The tone exits at U0103-23 and is routed to the audio PA like receive audio.

Midband SPECIFIC CIRCUIT DESCRIPTION

8.0 Receiver Front-End

The receiver is able to cover the MB range from 66 to 88 MHz. It consists of four major blocks: front-end, mixer, first IF section and IF IC. Antenna signal pre-selection is performed by two varactor tuned bandpass filters. A double balanced schottky diode mixer converts the signal to the first IF at 21.4MHz.

Two crystal filters in the first IF section and two ceramic filters in the second IF section provide the required selectivity. The second IF at 455 kHz is mixed, amplified and demodulated in the IF IC. The processing of the demodulated audio signal is performed by an audio processing IC located in the controller section.

8.1 Front-End Band-Pass Filter and Pre-Amplifier

A two pole pre-selector filter tuned by the dual varactor diode D2301 pre-selects the incoming signal (PA RX) from the antenna switch to reduce spurious effects to following stages. The tuning voltage (FE CNTL VLTG) ranging from 0.5 volts to 8 volts is controlled by a Digital to Analogue (D/A) converter (U0731-11) in the controller section. A dual hot carrier diode (D2303) limits any inband signal to 0dBm to prevent damage to the pre-amplifier.

The RF pre-amplifier is an SMD device (Q2301) with collector base feedback to stabilize gain, impedance, and intermodulation. The collector current of approximately 11-16 mA, drawn from the voltage 9V3 via L2302, is controlled by a current source composed of Q2302, R2302, R2300, and R2311 - R2313. In transmit mode the high K9V1 signal fed through diode D2300 switches off the current source and in turn the pre-amplifier. In receive mode K9V1 must be low to switch on the current source. A 3 dB pad (R2306 - R2308 and R2316 - R2318) stabilizes the output impedance and intermodulation performance.

A second two pole varactor tuned bandpass filter provides additional filtering to the amplified signal. The dual varactor diode D2304 is controlled by the same signal which controls the pre-selector filter.

If the radio is configured for a base station application, R2318 is not placed and TP2301 and TP2302 are shorted.

8.2 Mixer and Intermediate Frequency (IF) Section

The signal coming from the front-end is converted to the first IF (21.4 MHz) using a double balanced schottky diode mixer (D2331). Its ports are matched for incoming RF signal conversion to the 21.4MHz IF using high side injection. The injection signal (VCO MIXER) coming from the mixer buffer (Q2770) is filtered by the lowpass consisting of (L2333, L2334, C2331 - C2333, C2337) and has a level of approximately 10 dBm.

The mixer IF output signal (RX IF) from transformer T2301 pin 2 is fed to the first two pole crystal filter Y2201. The filter output in turn is matched to the following IF amplifier. The IF amplifier Q2201 is actively biased by a collector base feedback (R2201, R2202) to a current drain of approximately 1mA drawn from the voltage 5V STAB. Its output impedance is matched to the second two pole crystal filter Y2202. A dual hot carrier diode (D2201) limits the filter output voltage swing to reduce overdrive effects at RF input levels above -27 dBm.

8.3 IF IC (U2201)

The first IF signal from the crystal filters feeds the IF IC (U2201) at pin 6. Within the IF IC the 21.4MHz first IF signal mixes with the second local oscillator (LO) at 20.945MHz to the second IF at 455 kHz. The second LO uses the external crystal Y2211. The second IF signal is amplified and filtered by two external ceramic filters (FL2201, FL2202). Back in the IF IC the signal is demodulated in a phase-lock detector and fed from IF IC pin 28 to the audio processing circuit AFIC U0103 located in the controller section (line DET AUDIO).

The IF IC also controls the squelch characteristics of the radio. With a few external parts (R2221, R2222, C2225, C2226, C2229, C2230, R2223) the squelch tail, hysteresis, attack and delay were optimized for the radio. To set the squelch threshold the signal from IF IC pin 23 (line SQ ATT IN) is attenuated by a microprocessor controlled audio processing IC AFIC (U0103) located in the controller section. The attenuated signal from the AFIC (line SQ ATT OUT) enters the IF IC at pin 20 and is used to create a squelch indicator signal available at pin 15 (CSQ DET).

The microprocessor controlled ADAPT signal at pin 22 activates the fast squelch indicator signal at IF IC pin 18 (FAST SQ). Both squelch indicator signals CSQ DET (pin 15) and FAST SQ (pin 18) are combined, weighted by R0111 / R0112 and fed to the microprocessor U0101 pin 15 for interpretation. From the voltage weighted by the resistors the uP determines whether CSQ DET, FAST SQ or both are active.

At IF IC pin 11 an RSSI signal is available with a dynamic range of 70 dB. In 128 channel radios the RSSI signal is buffered by op-amp U0106-3 and available at accessory connector J0400-15 while in 4 channel radios the RSSI signal is fed unbuffered through R0153 to the accessory connector J0400-15.

9.0 Transmitter Power Amplifier (PA) 5-25W

The radio's 5-25 W PA is a three stage amplifier used to amplify the output from the exciter to the radio transmit level. It consists of the following stages in the line-up. The first (Q2511) is a bipolar stage that is controlled via the PA control line (line PWR CNTL). It is followed by a MOS FET stage (Q2521) and a final bipolar stage (Q2531).

Devices Q2511 and Q2521 are surface mounted. Bipolar Transistor Q2531 is directly attached to the heat sink.

9.1 Power Controlled Stage

The first stage (Q2511) amplifies the RF signal from the VCO (line EXCITER PA) and controls the output power of the PA. The output power of the transistor Q2511 is proportional to its collector current which is adjusted by a voltage controlled current source consisting of Q2641, Q2642 and Q2643. The current of the whole stage is drawn from the RX-TX Switch through coil L2652.

Transistor Q2643 , controlled by the microprocessor via signal K9V1, switches the current source on in transmit mode and off in receive mode.

The collector current of Q2511, drawn via L2641, causes a voltage drop across the resistors R2645 and R2646. Transistor Q2641 adjusts the voltage drop across R2644 controlled through the PA control line (PWR CNTL). The current source Q2642 adjusts the collector current of Q2511 by modifying its base voltage via R2601-R2603 until the voltage drop across R2645 and R2646 plus V_{BE} (0.6V) equals the voltage drop across R2644. If the voltage of PWR CNTL is raised, the base voltage of Q2641 will also rise causing more current to flow to the collector of Q2641 and a higher voltage drop across R2644. This in turn results in more current driven into the base of Q2511 by Q2642 so that the collector current of Q2511 is increased. The collector current settles when the voltage over the series configuration of R2645 and R2646 plus V_{BE} of Q2642 equals the voltage over R2644. By controlling the output power of Q2511 and in turn the input power of the following stages the ALC loop is able to regulate the output power of the transmitter.

In receive mode the PA control line (PWR CNTL) is at ground level and switches off the collector current of Q2641 which in turn switches off the current source transistor Q2642 and the RF transistor Q2511.

9.2 PA Stages

The following stage uses an enhancement mode N-Channel MOS FET device (Q2521) and requires a positive gate bias and a quiescent current flow for proper operation. The voltage of the line BIAS VLTG is set in transmit mode by a Digital to Analogue (D/A) converter (U0731-4) and fed to the gate of Q2521 via the resistive network R2513, R2614, R2615. The bias voltage is tuned in the factory. If the transistor is replaced, the bias voltage must be tuned with the Radio Service Software (RSS). Care must be taken, not to damage the device by exceeding the maximum allowed bias voltage. The collector current is drawn from the supply voltage A+ via L2622, L2523, L2524.

The final stage uses the bipolar device Q2531 and operates off the A+ supply voltage. For class C operation the base is DC grounded by two series inductors (L2521, L2522). A matching network consisting of C2530-C2534, L2532, L2533 and two striplines transforms the impedance to 50 Ohms and feeds the directional coupler.

9.3 Directional Coupler

The directional coupler is a microstrip printed circuit which couples a small amount of the forward power off the RF power from Q2531. The coupled signal is rectified to an output power proportional negative DC voltage by the diode D2657 and sent to the power control circuit in the controller section via the line PWR DETECT for output power control. The power control circuit holds this voltage constant, thus ensuring the forward power out of the radio to be held to a constant value.

9.4 Antenna Switch

The antenna switch is switched synchronously with the K9V1 voltage along with the voltage PWR CNTL signal and feeds either the antenna signal coming through the harmonic filter to the receiver or the transmitter signal coming from the PA to the antenna via the harmonic filter.

In transmit mode, this PWR CNTL voltage is above 1 V and biases Q2511 through Q2641 and Q2642 to allow a collector current to be drawn. The collector current of Q2511 drawn from A+ flows via L2631, L2531, L2533, directional coupler, D2551, L2651, D2651, L2652, R2645, R2646, L2641, and switches the PIN diodes D2551 and D2651 to the low impedance state. D2551 leads the RF signal from the directional coupler to the harmonic filter. The low impedance of D2651 is transformed to a high impedance at the input of the harmonic filter by the resonant circuit formed by L2651,C2652 and the input capacitance of the harmonic filter.

Transistor Q2643, controlled by the microprocessor via Signal K9V1, is used to switch the collector current of Q2641 on in transmit mode and off in receive mode. In receive mode the low K9V1 and the low PWR CNTL turn off the collector current of Q2511 through Q2641 and Q2642. With no current drawn by Q2511 and resistor R2651 pulling the voltage at PIN diode D2651 to A+ both PIN diodes are switched to the high impedance state. The antenna signal, coming through the harmonic filter, is channelled to the receiver via L2651, C2651 and line PA RX. The high impedance of D2551/ D2651 in off state does not influence the receiver signal.

9.5 Harmonic Filter

The transmitter signal from the antenna switch is channelled through the harmonic filter to the antenna connector J2501.The harmonic filter is formed by inductors L2550 - L2553, and capacitors C2551 through to C2554 This network forms a low-pass filter to attenuate harmonic energy of the transmitter to specifications level. R2551 is used for electro-static protection.

9.6 Power Control

The power control loop regulates transmitter power with an automatic level control (ALC) loop and provides protection features against excessive control voltage and high operating temperatures.

MOS FET device bias, power and control voltage limit are adjusted under microprocessor control using a Digital to Analogue (D/A) converter (U0731). The microprocessor writes the data into the D/ A converter via serial interface (SRL) composed of the lines SPI CLCK SRC (clock), SPI DATA SRC (data) and DAC CE (chip enable). The D/A adjustable control voltage limit increases transmitter rise time and reduces adjacent channel splatter as it is adjusted closer to the actual operating control voltage.

The microprocessor controls K9V1 ENABLE (U0101-6) to switch on the first PA stage via transistors Q0741, Q0742 and signal K9V1. The antenna switch is turned on by the collector current of the first PA stage. PA DISABLE, also microprocessor controlled (U0101-54), sets BIAS VLTG (U0731-4) and VLTG LIMIT SET (U0731-13) via Q0731, D0731 in receive mode to low to switch off the bias of the MOS FET device Q2521 and to switch off the power control voltage (PWR CNTL).

Through an Analogue to Digital (A/D) input (VLTG LIMIT) the microprocessor can read the PA control voltage (PWR CNTL) during the tuning process.

The ALC loop regulates power by adjusting the PA control line PWR CNTL to keep the forward power voltage PWR DETECT at a constant level.

Opamp U0701-2 and resistors R0701 to R0703 and R0731 subtract the negative PWR DETECT voltage from the PA PWR SET D/A output U0731 pin 2. The result is connected to opamp inverting input U0701-4 pin 9 which is compared with a 4.6 volt reference VAG present at noninverting input U0701-4 pin 10 and controls the output power of the PA via pin 8 and control line PWR CNTL. The 4.6 volt reference VAG is set by a resistive divider circuit (R0171, R0172) which is connected to ground and 9.3 volts and buffered by opamp U0105-1.

During normal transmitter operation the voltages at the opamp inputs U0701-4 pins 9 and 10 should be equal to 4.6 volts and the PA control voltage output at pin 8 should be between 4 and 7 volts. If power falls below the desired setting, PWR DETECT becomes less negative, causing the output at U0701-2 pin 7 to decrease and the opamp output U0701-4 pin 8 to increase.

A comparator formed by U0701-4 increases the PA control voltage PA CNTL until PWR DETECT is at the desired level. The power set D/A output voltage PWR SET (U0731-2) at U0701-2 pin 5 adjusts power in steps by adjusting the required value of PWR DETECT. As PWR SET (U0731-2) decreases, transmitter power must increase to make PWR DETECT becomes more negative and keep the inverting input U0701-4 pin 9 at 4.6 volts.

Loop frequency response is controlled by opamp feedback components R0712 and C0711. Opamp U0701-3 compares the power control voltage PWR CNTL divided by resistors R0717 to R0719 with the voltage limit setting VLTG LIMIT SET from the D/A converter (U0731-13) and keeps the control voltage constant via Q0711 if the control voltage, reduced by the resistive divider (R0717 to R0719), approaches the voltage of VLTG LIMIT SET (U0731-13).

Rise and fall time of the output power during transmitter keying and dekeying is controlled by the comparator formed by opamp U0701-3.

During normal transmitter operation the voltage at U701-3 pin 13 is higher than the voltage at pin 12 causing the output at pin 14 being low and switching off transistor Q0711. Diode D0732 reduces the bias voltage BIAS VLTG for low control voltage levels.

The temperature of the PA area is monitored by opamp U0701-1 using thermistor R2611 (located in the PA section). If the temperature increases, the resistance of the thermistor decreases, decreasing the voltage PA TEMP. The inverting amplifier formed by U0701-1 amplifies the PA TEMP voltage and if the voltage at opamp pin 1 approaches 4.6 V plus the voltage (ON) across D0721, U701-1 simulates an increased power which in turn decreases the power control voltage until the voltage at U0701-4 pin 9 is 4.6V again. Resistor R0724, R0722, R0723 set the factor of the decrease in output power per temperature increase while R0721 through R0723 set the threshold were the temperature starts reducing the output power. During normal transmitter operation the output voltage of opamp U701-1 pin 1 is below 4.6V. Diode D2601 located in the PA section acts as protection against transients and wrong polarity of the supply voltage.

10.0 Frequency Synthesis

The complete synthesizer subsystem consists of the Reference Oscillator (Y2701 or Y2702), the Fractional-N synthesizer (U2701), the Voltage Controlled Oscillator (Q2741, Q2751), the RX and TX buffer stages (Q2760, Q2770, Q2780) and the feedback amplifier (Q2790).

10.1 Reference Oscillator

The Reference Oscillator (Y2702) contains a temperature compensated crystal oscillator with a frequency of 16.8 MHz. An Analogue to Digital (A/D) converter internal to U2701 and controlled by the microprocessor via serial interface (SRL) sets the voltage at the warp output of U2701 pin 16 to set the frequency of the oscillator. The output of the oscillator (pin 2 of Y2702) is applied to pin 14 (XTAL1) of U2701 via a RC series combination.

In applications were less frequency stability is required the oscillator inside U2701 is used along with an external crystal Y2701, the varactor diode D2702, C2708, C2710 and R2704. The crystal may not be replaced in case of failure. Instead of the crystal, the reference oscillator Y2702 must be soldered in along with C2706, C2707, R2703. Components Y2701, C2708, C2710, R2704, D2702 must be removed and the value of C2709 must be changed. Afterwords the radio must be retuned.

10.2 Fractional-N Synthesizer (U2701)

The FRAC-N synthesizer IC (U2701) consists of a pre-scaler, a programmable loop divider, control divider logic, a phase detector, a charge pump, an A/D converter for low frequency digital modulation, a balance attenuator to balance the high frequency analogue modulation and low frequency digital modulation, a 13V positive voltage multiplier, a serial interface for control, and finally a super filter for the regulated 9.3 volts.

A voltage of 9.3V applied to the super filter input (U2701 pin 19) supplies an output voltage of 8.6VDC at pin 18. It supplies the VCO (Q2741 / Q2751), VCO modulation bias circuit (R2714) and the synthesizer charge pump resistor network (R2723, R2724). The synthesizer supply voltage is provided by the 5V regulator U2801.

In order to generate a high voltage to supply the phase detector (charge pump) output stage at pin VCP (U2701-32), a voltage of 13 VDC is being generated by the positive voltage multiplier circuitry (D2701-1-3, C2716, C2717). This voltage multiplier is basically a diode capacitor network driven by two (1.05 MHz) 180 degrees out of phase signals (U2701-9 and -10).

Output LOCK (U2701-2) provides information about the lock status of the synthesizer loop. A high level at this output indicates a stable loop. IC U2701 divides the 16.8MHz reference frequency down to 2.1MHz and provides it at pin 11. This signal is used as clock signal by the controller.

The serial interface (SRL) is connected to the microprocessor via the data line SPI DATA (U2701-5), clock line SPI CLK (U2701-6), and chip enable line FRACN CE (U2701-7).

10.3 Voltage Controlled Oscillator (VCO)

The Voltage Controlled Oscillator (VCO) uses 2 colpitts oscillators, FET Q2741 for transmit and FET Q2751 for receive. The appropriate oscillator is switched on or off by FRAC-N IC output AUX3 (U2701-1) using transistors Q2742 and Q2752. In RX mode AUX3 is nearly at ground level and Q2742 enables a current flow from the source of FET Q2751 while Q2752 is switched off. In TX mode AUX3 is about 5V DC and Q2742 is switched off. Q2752 is switched on and enables a current flow from the source of FET Q2741 while Q2751 is switched off. When switched on the FETs draw a drain current of 8 mA from the FRAC-N IC super filter output. The frequency of the receive oscillator is mainly determined by L2752, L2753, C2752 - C2756 and varactor diodes D2751 / D2752. Diode D2754 controls the amplitude of the oscillator. The frequency of the transmit oscillator is mainly determined by L2734, C2736 - C2740 and varactor diodes D2732 / D2733. Diode D2739 controls the amplitude of the oscillator. With a steering voltage from 3V to 10V at the varactor diodes the RX frequency range from 87.4MHz to 109.4MHz and the TX frequency range from 66MHz to 88MHz are covered. In TX mode the modulation signal coming from the FRAC-N synthesizer IC (U2701 pin 28) modulates the TX VCO via varactor diode D2731.

Both oscillator outputs are combined and buffered by the VCO Buffer Q2760. Q2760 draws a collector current of 13 mA from the stabilized 5V (U2801) and drives the Mixer Buffer Q2770. Q2770 draws a collector current of 19 mA from the 9V3 voltage and drives the PA Buffer Q2780 (Pout = 13dBm) and the Pre-scaler Buffer Q2790. Q2790 draws a collector current of 8 mA from the stabilized 5V (U2801) and drives the pre-scaler internal to the FRAC-N IC. In transmit mode Q2780 is switched on by the K9V1 signal and draws a collector current of 19 mA from the K9V1 voltage. The injection signal VCO MIXER with a level of 10dBm feeds the mixer through R2774. The buffer stages Q2760, Q2770, Q2780 and the feedback amplifier Q2790 provide the necessary gain and isolation for the synthesizer loop.

10.4 Synthesizer Operation

The complete synthesizer subsystem works as follows. The combined output signal of the RX VCO (Q2751) and TX VCO (Q2741) is buffered by VCO Buffer Q2760, Mixer Buffer Q2770 and Pre-scaler Buffer Q2790. To close the synthesizer loop, the collector of Q2790 is connected to the PREIN port of synthesizer U2701 (pin 20). The output of the VCO Buffer (Q2770) also provides signals for the mixer (via VCO MIXER) and the PA Buffer (Q2780).

The pre-scaler in the synthesizer (U2701) is basically a dual modulus pre-scaler with selectable divider ratios. This divider ratio of the pre-scaler is controlled by the loop divider, which in turn receives its inputs via the SRL. The output of the pre-scaler is applied to the loop divider. The output of the loop divider is connected to the phase detector, which compares the loop divider´s output signal with the reference signal.The reference signal is generated by dividing down the signal of the reference oscillator (Y2701 or Y2702).

The output signal of the phase detector is a pulsed DC signal which is routed to the charge pump. The charge pump outputs a current at pin 29 (I OUT of U2701). The loop filter (which consists of R2715 - R2718, C2723 - C2725, C2727, C2735) transforms this current into a voltage that is applied to the varactor diodes D2732, D2733 (TX), D2751, D2752 (RX) and alters the output frequency of the TX VCO (Q2741) and RX VCO (Q2751). The current can be set to a value fixed in the FRAC-N IC or to a value determined by the current flowing into CPBIAS 1 (U2701-27). The current is set by the value of R2723 and R2724. The selection of the two different bias sources is done by software programming.

To reduce synthesizer lock time when new frequency data has been loaded into the synthesizer the magnitude of the loop current is increased by enabling the IADAPT line (U2701-31) for a certain software programmable time (Adapt Mode). The adapt mode timer is started by a low to high transient of the FRACN CE line. When the synthesizer is within the lock range the current is determined only by the resistors connected to CPBIAS 1 or the internal current source. A settled synthesizer loop is indicated by a high level of signal LOCK DET (U2701-2). This signal is routed to µP U0101-17 for further processing.

In order to modulate the PLL the two spot modulation method is utilized. Via pin 8 (MODIN) on U2701 the audio signal is applied to both the A/D converter (low freq path) as well as the balance attenuator (high freq path). The A/D converter converts the low frequency analogue modulating signal into a digital code that is applied to the loop divider, thereby causing the carrier to deviate. The balance attenuator is used to adjust the VCO’s deviation sensitivity to high frequency modulating signals. The output of the balance attenuator is present at the MODOUT port (U2701-28) and connected to the VCO modulation diode D2731 via L2731, C2733.

Chapter 7.4

66-88MHz Diagrams and Parts Lists

Table of Contents

Description Page

Midband (66-88MHz) Diagrams and Parts Lists

PCB Layout Component Side 1
PCB Layout Solder Side 2
128ch Model, Controller Schematic Diagram *1 of 2* 3
128ch Model, Controller_IO Schematic Diagram *2 of 2* 5
Parts List 4/6
4ch Model, Controller Schematic Diagram *1 of 2* 7
4ch Model, Controller_IO Schematic Diagram *2 of 2* 9
Parts List 8/10
Supply Voltage Schematic Diagram. 11
Parts List 12
Power Control Schematic Diagram 13
Parts List 14
Power Amplifier 5-25W Schematic Diagram 15
Parts List 16
Synthesizer Schematic Diagram 17
Parts List 18
Voltage Controlled Oscillator Schematic Diagram 19
Parts List 20
RX-FE Schematic Diagram 21
Parts List 22
RX-IF Schematic Diagram 23
Parts List 24

Appendix A

PL/DPL Codes

Table of Contents

Paragraph Page

1.0 PL Codes and Digital PL (DPL) Codes 1

2.0 Self-Quieting Frequencies 1

1.0 PL Codes and Digital PL (DPL) Codes

The following PL Codes have been tested and are acceptable for programming into any transmit or receive frequency.

GROUP A		GROUP B		GROUP C	
Code	**Freq**	**Code**	**Freq**	**Code**	**Freq**
XZ	67.0	XA	71.9	WZ	69.3
XB	77.0	YZ	82.5	WA	74.4
YB	88.5	ZA	94.8	WB	79.7
1Z	100.0	1A	103.5	YA	85.4
1B	107.2	2Z	110.0	ZZ	91.5
2A	114.8	2B	118.8	ZB	97.4
3Z	123.0	3A	127.3	5B	162.2
3B	131.8	4Z	136.5	8Z	206.5
4A	141.3	4B	146.2		
5Z	151.4	5A	156.7		
6A	173.8	6Z	167.9		
7Z	186.2	6B	179.9		
M1	203.5	7A	192.8		
M3	218.1	M2	210.7		

Digital PL (DPL) Codes:

023	025	026	031	032	036
043	047	051	053	054	065
071	072	073	074	114	115
116	122	125	131	132	134
143	145	152	155	156	162
165	172	174	205	212	223
225	226	243	244	245	246
251	252	255	261	263	265
266	271	274	306	311	315
325	331	332	343	346	351
356	364	365	371	411	412
413	423	431	432	445	446
452	454	455	462	464	465
466	503	506	516	523	526
532	546	565	606	612	624
627	631	632	654	662	664
703	712	723	731	732	734
743	754				

2.0 Self-Quieting Frequencies

Self-quieting frequencies are frequencies that are also generated by the radio and cause internal interference. On these frequencies the interference caused by the self-quieter spur is great enough that a radio will not meet its receiver sensitivity specification.

The frequencies are: UHF 403.2, 420, 436.8 and 453.6MHz.
VHF 151.2 and 168.0MHz

Appendix B

External Device Connectors

Table of Contents

Paragraph Page

1.0 Accessory Connector Details 1

2.0 Microphone Connector 3

1.0 Accessory Connector Details

The 16-pin accessory connector pin functions are as follows:

Pin	Name	Type	A2 4-Channel	A3 128-Channel
1	SPKR-	Analogue output	✓	✓
2	Ext. Mic Audio	Analogue input	✓	✓
3	GP1	Digital input	✓	✓
4	GP2	Digital output	✕	✓
5	Flat TX Audio	Analogue input	✕	✓
6	BUS+	Digital i/o	✓	✓
7	GND	Ground	✓	✓
8	GP3	Digital i/o	✕	✓
9	GP4	Digital ip. capture	✕	✓
10	Ignition sense	Digital input	✓	✓
11	RX Audio	Analogue output	✕	✓
12	GP5	Digital i/o	✕	✓
13 *	SW B+ / GND	Analogue output	✕	✓
14	GP6	Digital i/o	✕	✓
15	RSSI	Analogue output	✓ **(Unbuffered)**	✓
16	SPKR+	Analogue output	✓	✓

* Factory default SWB+.

Pin 1. - **Speaker - audio**
Speaker - and Speaker + (Pin 16) are used to connect an external speaker. The audio PA is a bridge amplifier with a minimum load resistance of 3.2 ohms. The internal speaker can be disabled by removing the control head. Disconnect the internal speaker and assemble the control head back to the radio.

Pin 2. - **Microphone audio**
This microphone signal input is common with the microphone signal input on the microphone connector and is connected to the microphone path input of the AFIC. The nominal input level is 80mV for 60% deviation. The DC impedance is 1100 ohms and the AC impedance is 1000 ohms
Note: Only one microphone should be connected at any one time.

Pin 3. - **General Purpose 1 (GP 1)**
This is a digital input only. The RSS details which functions may be assigned to this pin by the codeplug. The primary use for this pin will be external PTT. (See Note 1).

Pin 4. - **General purpose 2 (GP2)**
This is a digital output only. The RSS details which functions may be assigned to this pin by the codeplug. The primary use for this pin is as external alarm output (See Note 3).

Pin 5. - **Flat TX audio**
This input is for injecting signals into the transmit path that should not be filtered, e.g. the output of a modem. The nominal input level is 150mVRMS for 60% deviation. The impedance is greater than 25kohms.

Pin 6. - **BUS+**
This connects to the radio's SCI serial bus which is used for programming and tuning the radio. The line is also available at the microphone connector Pin 7.

Pin 7. - **Ground**
Used as ground for both analogue and digital signals.

Pin 8. - **General purpose 3 (GP3)**
This is a digital input/output and is also available on the internal option connector (J0103:7). The RSS details which functions may be assigned to this pin by the codeplug. (See Notes 1 and 2).

Pin 9. - **General purpose 4 (GP4)**
This is a digital input only. It is also available on the internal option connector (J0102:7) and is used in input capture mode when a serial type option board is fitted. The RSS details which functions may be assigned to this pin by the codeplug. (See Note 1).

Pin 10. - **Ignition sense**
Connecting this line to the ignition line of the vehicle will automatically turn the radio on when the ignition of the vehicle is turned on. When ignition is connected, the radio cannot be turned off as long as the ignition is active. When this line is at 0V or not connected, power on/off is under manual control. Resistor R0423, 4.7kΩ, which is not fitted as standard will cause the radio to be permanently on whenever 12V is connected to the main power connector.

Pin 11. - **RX Audio Discriminator/Filtered (Analogue output)**
The signal routed to this pin is controlled by AFIC. There are two possible outputs; continuous discriminator audio or continuous filtered RX audio output of AFIC. The output mode can be selected by the RSS, however, this mode may be overridden during certain tuning operations. For discriminator audio, the nominal ouput level is 330mVRMS for 60% deviation. The impedance is 600ohms. For filtered audio, the nominal ouput level is 600mV for 60% deviation. The impedance is 600ohms.

Pin 12. - **General purpose 5 (GP5)**
This is a digital input/output and is also available on the internal option connector (J0103:8). The RSS details which functions may be assigned to this pin by the codeplug. (See Notes 1 and 2).

Pin 13. - **Switched B+ / Analogue Ground**
The output of this pin may be configured by a solder link within the radio. Switched B+ is the default. The current limiting resistor (R0455) default is 0Ω, therefore extreme care must be taken to avoid short circuiting this output to ground, which will damage the radio.

CAUTION: The maximum continuous current allowed is 300mA. A suitable external fuse must be installed into the lead to pin 13 to avoid damage to the radio.



Pin 14. - **General purpose 6 (GP6)**
This is a digital input/output and is also available on the internal option connector (J0102:3). The RSS details which functions may be assigned to this pin by the codeplug. (See Notes 1 and 2).

Pin 15. - **RSSI**
Received Signal Strength Indication, buffered analogue voltage.

Pin 16. - **Speaker+ audio**
Positive output of radio's audio PA (see Pin 1).

Note 1: **Digital Input**
4.7 kΩ Internal Pull Up Resistor to +5V.
Maximum Input Voltage accepted as Low = 0.6V
Minimum Input Voltage accepted as High = 3.0V

Note 2: **Digital Output**
4.7kΩ Internal Pull Up Resistor to +5V
Maximum Current when Output Low = 10mA
Maximum Voltage when Output Low = 0.5V @ 10mA

Note 3: **High Current Digital Output**
4.7kΩ Internal Pull Up Resistor to B+
Maximum Current when Output Low = 200mA
Maximum Voltage when Output Low = 1.7V @200mA

2.0 Microphone Connector

The radio is fitted with an 8-pin ‘Telco’ connector which is connected as follows:

Pin	Name	Type	Connected To
1	-	-	-
2	-	-	-
3	Mic. Hook	Digital input	Port A7
4	GND	Ground	-
5	Mic. Audio	Analogue input	AFIC TX IN
6	Mic. PTT	Digital i/o	Port C4
7	BUS+	Digital i/o	Port D0 and Port D1
8	HANDSET	Analogue output	Buffered RX audio

Pin 1. - No connection.

Pin 2. - No connection.

Pin 3. - **Microphone (or internal) Hook**
This port reads ‘0’ when the microphone is on-hook and ‘1’ when the microphone is off-hook. It is assumed that the hook is a mechanical switch, so the software will always debounce this input.

Pin 4. - **Ground**

Pin 5. - **Microphone audio**
This microphone signal input is common with the microphone signal input on the accessory connector and is connected to the microphone path input of the AFIC.
Note: Only one microphone should be connected at any one time.

Pin 6. - **Microphone (or Internal) PTT**
The microphone PTT is active low and so this port reads ‘0’ when the PTT is pressed and ‘1’ when the PTT is released. It is assumed that this PTT is a mechanical switch, so the software will always debounce this input.

The microphone PTT line is also available at the internal connector (J0102:1) as a bi-directional line, i.e. an internal option can use the line, both to key-up the radio, and to know when the radio is already keyed-up. For this to work, microprocessor port C4 has to be reconfigured as an output and driven low whenever any other signal, other than the microphone PTT, e.g. external PTT, causes the radio to key-up.

Pin 7. - **BUS+**
This line carries the data for the single line serial comms system used in the radio. The RSS will program the radio through this socket. The line is also available at the accessory connector Pin 6.

Pin 8. - **Handset Audio**
This line provides buffered audio for a handset.

Appendix C

Radio Conversion

Table of Contents

Paragraph Page

1.0 How to alter the radio for Base Station Operation 1

1.0 How to alter the radio for Base Station Operation

UHF Radio Conversion
If the UHF radio is configured for a base station application, R5319 is not placed and TP5301 and TP5302 are shorted.

VHF Radio Conversion
If the VHF radio is configured for a base station application, R3318 is not placed and TP3301 and TP3302 are shorted.